

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X2523 MLB_S

LAST MODIFICATION= Tue May 31 17:07:36 2022

PAGE	CSA	CONTENTS	SYNC	DATE
1	1	Table of Contents		
2	2	REFERENCE DESIGN TABLE		06/28/2021
3	4	PD PARTS		08/24/2021
4	5	SOC: CONFIG STRAPS	T585_REF_SOC_H148_0.16.0	
5	6	SOC: RESETS, CLOCKS, SWD	T585_REF_SOC_H148_0.16.0	
6	8	SOC: GPIO, I2C, I2S, SEI, UART	T585_REF_SOC_H148_0.16.0	
7	10	SOC: CONFIG STRAPS	T585_REF_SOC_H148_0.16.0	
8	12	SOC: PCIe	T585_REF_SOC_H148_0.16.0	
9	14	SOC: CIO, USB	T585_REF_SOC_H148_0.16.0	
10	16	SOC: AOP, SMC, NUB	T585_REF_SOC_H148_0.16.0	
11	19	SOC: SHARED SUPPORT	J414_DTUZYMAN_MLB_S_0.61.1	
12	20	SOC: SPI NOR, SEP ROM, LPS RESET	T585_REF_SOC_H148_0.16.0	
13	21	PROJECT SUPPORT (1/2)	J414_MIRABEAU_MLB_S_0.11.1 08/12/2021	
14	22	PROJECT SUPPORT (2/2)	T585_REF_SOC_H148_0.16.0	
15	23	SOC: POWER (CPU, GPU)	T585_REF_SOC_H148_0.16.0	
16	25	SOC: POWER (SRAM, DISP, DCS)	T585_REF_SOC_H148_0.16.0	
17	27	SOC: POWER (VDD1)	T585_REF_SOC_H148_0.16.0	
18	29	SOC: POWER (VDDQ)	T585_REF_SOC_H148_0.16.0	
19	31	SOC: POWER (APR, ANE, CIO)	T585_REF_SOC_H148_0.16.0	
20	33	SOC: POWER (FABRIC, FIXED)	T585_REF_SOC_H148_0.16.0	
21	35	SOC: POWER (VDDIO)	T585_REF_SOC_H148_0.16.0	
22	37	SOC: POWER (VDD2H0)	T585_REF_SOC_H148_0.16.0	
23	39	SOC: POWER (VDD2H1)	T585_REF_SOC_H148_0.16.0	
24	41	SOC: GND-1	T585_REF_SOC_H148_0.16.0	
25	42	SOC: GND-2	T585_REF_SOC_H148_0.16.0	
26	43	SOC: GND-3	T585_REF_SOC_H148_0.16.0	
27	50	Secure Element	T585_REF_SE_EOS_0.2.2	
28	51	BATTERY CONN		08/12/2021
29	52	PMU SUPPLY & BATTERY CHARGER	T585_REF_CHARGER_MIRABEAU_S_0.16.0 02/10/2022	
30	53	BATTERY CHARGER SUPPORT	T585_REF_CHARGER_MIRABEAU_S_0.16.0	
31	54	MAGSAFE: CONNECTOR	J414_DTUZYMAN_MLB_S_0.16.1	
32	55	MAGSAFE: PORT CONTROLLER	T585_REF_MAGSAFE_ACR2_20V_0.4.27	
33	56	MAGSAFE: CONTROLLER SUPPORT		08/12/2021
34	57	POWER: 3V8 AON (1/2)	T585_REF_VR_ICEMAN_1.46.0	
35	58	POWER: 3V8 AON (2/2)	T585_REF_VR_ICEMAN_1.46.0	
36	60	POWER: 3V8 AON OUTPUT THROTTLE	T585_REF_VR_ICEMAN_H08/12/2021	
37	76	PMU OUTPUT DESENSE CAPS	T585_REF_PMIC_MAVRICKS_H14_0.36.0	
38	77	SPMU VIN/LDO/SW	T585_REF_PMIC_MAVRICKS_H14_0.36.0	
39	78	SPMU BUCKS	T585_REF_PMIC_MAVRICKS_H14_0.36.0	
40	79	SPMU GPIO & GND	T585_REF_PMIC_MAVRICKS_H14_0.36.0	
41	80	PMU BUCK OUTPUT CAPS	T585_REF_PMIC_MAVRICKS_H14_0.36.0	
42	81	MPMU VIN/LDO/SW	T585_REF_PMIC_MAVRICKS_H14_0.36.0	
43	82	MPMU BUCKS	T585_REF_PMIC_MAVRICKS_H14_0.36.0	
44	83	MPMU GPIO & GND	T585_REF_PMIC_MAVRICKS_H14_0.36.0	
45	84	PMU PROJECT-SPECIFIC SUPPORT	T585_REF_VR_AUSTRINGER_0.34.0	
46	85	PMU PROJECT-SPECIFIC SUPPORT 2	J414_MLB_S_0.17.0 09/13/2021	
47	92	AUSTRINGER SUPPORT	J414_MLB_S_1.18.0	
48	93	AUSTRINGER CONTROLLER	T585_REF_VR_AUSTRINGER_0.34.0	
49	94	AUSTRINGER POWER STAGES 1	T585_REF_VR_AUSTRINGER_0.34.0	
50	95	AUSTRINGER POWER STAGES 2	T585_REF_VR_AUSTRINGER_0.34.0	
51	101	CLVR0	T585_REF_CLVR_MIRABEAU_0.30.0	
52	102	CLVR1	T585_REF_CLVR_MIRABEAU_0.30.0	
53	106	CLVR2 (S)	T585_REF_CLVR_MIRABEAU_0.30.0	
54	118	CLVR PROJECT SUPPORT (S)	T585_REF_CLVR_MIRABEAU_0.30.0	
55	122	POWER: 5V S2	T585_REF_VR_S2_S2621371_0.9.0	
56	130	I2C Connections - AP	J416_MLB_C_0.11.0 08/12/2021	
57	131	I2C Connections - SMC	J416_MLB_C_0.11.0 08/12/2021	
58	132	I2C Connections - Other	J414_HUKRATI_MLB_S_1.7.1	
59	135	SENSORS: HIGH-SIDE (1/3)	J414_HUKRATI_MLB_S_1.14.2	
60	136	SENSORS: HIGH-SIDE (2/3)	J414_HUKRATI_MLB_S_1.14.2	

LAST MODIFICATION= Tue May 31 17:07:36 2022

PAGE	CSA	CONTENTS	SYNC	DATE
61	137	SENSORS: HIGH-SIDE (3/3)	J414_HUKRATI_MLB_S_1.14.2	
62	138	SENSORS: LOW-SIDE (1/3)	J414_HUKRATI_MLB_S_1.14.2	
63	139	SENSORS: LOW-SIDE (2/3)	J414_HUKRATI_MLB_S_1.14.2	
64	140	SENSORS: LOW-SIDE (3/3)	J414_MLB_C_0.116.0	
65	141	SENSORS: THERMAL	J414_MLB_C_0.116.0	
66	144	SENSORS: MOTION	T585_REF_IMU_SOVEREIGN_0.15.0	
67	145	FANS	J414_MLB_C_2.33.0	
68	147	USB-C: Left Connectors	J414_RUENJOU_MLB_C_0.09/12/2021	
69	149	USB-C: Right Connector	J414_RUENJOU_MLB_C_0.09/12/2021	
70	150	USB-C: High Speed ATCO	T585_REF_USB_C_H148_0.16.0 02/01/2022	
71	151	USB-C: High Speed ATC1	T585_REF_USB_C_H148_0.16.0 02/01/2022	
72	152	USB-C: Support 1 ATC01	T585_REF_USB_C_H148_0.16.0 02/01/2022	
73	153	USB-C: Support 2 ATC01	T585_REF_USB_C_H148_0.16.0 02/01/2022	
74	154	USB-C: Port Controller ATCO	T585_REF_USB_C_H148_0.16.0 02/15/2022	
75	155	USB-C: Port Controller ATC1	T585_REF_USB_C_H148_0.16.0 02/15/2022	
76	156	USB-C: USB2 RPT	T585_REF_USB_C_H148_0.16.0 05/09/2022	
77	157	USB-C: HS Level Shifters ATC01	T585_REF_USB_C_H148_0.16.0 02/01/2022	
78	158	USB-C: 5V Regulator	T585_REF_USB_C_H148_0.16.0 02/01/2022	
79	159	USB-C: ATC01 REGULATORS	T585_REF_VR_VR13_PORTABLES_0.13.0	
80	160	USB-C: High Speed ATC2	T585_REF_USB_C_H148_0.16.0 02/01/2022	
81	162	USB-C: Support 1 ATC2	T585_REF_USB_C_H148_0.16.0 02/01/2022	
82	163	USB-C: Support 2 ATC2	T585_REF_USB_C_H148_0.16.0 02/15/2022	
83	164	USB-C: Port Controller ATC2	T585_REF_USB_C_H148_0.16.0 02/15/2022	
84	166	USB-C: USB2 RPT2	T585_REF_USB_C_H148_0.16.0 02/01/2022	
85	167	USB-C: HS Level Shifters ATC2	T585_REF_USB_C_H148_0.16.0 02/01/2022	
86	168	USB-C: 5V Regulator	T585_REF_USB_C_H148_0.16.0 02/15/2022	
87	169	USB-C: ATC2 REGULATORS	T585_REF_VR_VR13_PORTABLES_0.13.0	
88	170	USB-C: SUPPORT	J414_RUENJOU_MLB_C_0.16.2 08/12/2021	
89	175	HDMI: CONNECTOR	T585_REF_HDMI_COBRA_0.45.0 04/22/2022	
90	176	HDMI: DESENSE FILTERS	T585_REF_HDMI_COBRA_0.45.0 04/22/2022	
91	177	HDMI: COBRA	T585_REF_HDMI_COBRA_0.45.0 04/22/2022	
92	178	HDMI: Project Support 1	T585_REF_HDMI_COBRA_0.45.0 04/22/2022	
93	179	HDMI: Project Support 2	T585_REF_HDMI_COBRA_0.45.0 04/22/2022	
94	195	SDCARD CONTROLLER	T585_REF_SDCARD_GL9755_V2_0.7.0	
95	196	SDCARD CONNECTOR	T585_REF_SDCARD_GL9755_V2_0.7.0	
96	197	SDCARD IO L8/BUF SUPPORT	T585_REF_SDCARD_GL9755_V2_0.7.0	
97	198	SDCARD POWER SUPPORT	T585_REF_SDCARD_GL9755_V2_0.7.0	
98	200	WiFi/BT: MODULE	T585_REF_WIRELESS_WILLAMETTE_0.26.0	
99	201	WiFi/BT: ANTENNA AND GND	T585_REF_WIRELESS_WILLAMETTE_0.26.0	
100	220	STORAGE: SSD0 S5E M02 <0>	T585_REF_STORAGE_S5E_MARK2_0.14.0	
101	221	STORAGE: SSD0 S5E M02 <1>	T585_REF_STORAGE_S5E_MARK2_0.14.0	
102	222	STORAGE: SSD0 S5E M02 <2>	T585_REF_STORAGE_S5E_MARK2_0.14.0	
103	223	STORAGE: SSD0 S5E M02 <3>	T585_REF_STORAGE_S5E_MARK2_0.14.0	
104	224	STORAGE: SSD0 OCARINA & NAND VCC	T585_REF_STORAGE_S5E_MARK2_0.14.0	
105	225	STORAGE: SSD1 S5E M02 <0>	T585_REF_STORAGE_S5E_MARK2_0.14.0	
106	226	STORAGE: SSD1 S5E M02 <1>	T585_REF_STORAGE_S5E_MARK2_0.14.0	
107	227	STORAGE: SSD1 S5E M02 <2>	T585_REF_STORAGE_S5E_MARK2_0.14.0	
108	228	STORAGE: SSD1 S5E M02 <3>	T585_REF_STORAGE_S5E_MARK2_0.14.0	
109	229	STORAGE: SSD1 OCARINA & NAND VCC	T585_REF_STORAGE_S5E_MARK2_0.14.0	
110	230	STORAGE: SSD SUPPORT	T585_REF_STORAGE_S5E_MARK2_0.14.0 08/12/2021	
111	232	CAMERA-SUPPORT	J414_TERRILL_MLB_S_0.16.1 08/12/2021	
112	234	CAMERA: FLEX CONNECTOR	J414_TERRILL_MLB_S_0.16.1	
113	236	DISPLAY CONNECTOR	T585_REF_PANELPWR_20_6.4.008/12/2021	
114	237	DISPLAY POWER SEQUENCER	T585_REF_PANELPWR_20_6.4.008/12/2021	
115	238	LUXE LCD Backlight Driver	T585_REF_PANELPWR_20_6.4.008/12/2021	
116	239	BCON CONNECTOR	T585_REF_PANELPWR_20_6.4.008/12/2021	
117	242	SECDS: LID ANGLE SENSOR	T585_REF_SECDS_LAS_H14X_0.3.0	
118	243	SECDS: SAK	T585_REF_SECDS_LAS_H14X_0.3.0	
119	245	AUDIO JACK CODEC	T585_REF_CODEC_CARLOW_1.6.0	
120	246	AUDIO AMPLIFIERS (1/2)	T585_REF_SPKRAMP_S012776_3.8.0	

LAST MODIFICATION= Tue May 31 17:07:36 2022

PAGE	CSA	CONTENTS	SYNC	DATE
121	247	AUDIO AMPLIFIERS (2/2)	T585_REF_SPKRAMP_S012776_3.8.0	
122	248	AUDIO CONNECTORS: AMPS	T585_REF_IPD_0.30.0 08/12/2021	
123	249	AUDIO FLEX CONNECTORS	J414_MIRABEAU_MLB_S_0.11.1 08/12/2021	
124	250	BEN: KEYBD BKLT	T585_REF_BLC_BEN_KBD_ONLY_0.7.0	
125	251	KEYBOARD IOX, SUPPORT	T585_REF_IPD_0.30.0	
126	252	KEYBOARD SIGNAL CONNECTOR, RSD	T585_REF_IPD_0.30.0	
127	253	TRACKPAD SUPPORT 1	T585_REF_IPD_0.30.0	
128	254	TRACKPAD SUPPORT 2	T585_REF_IPD_0.30.0	
129	255	TOUCHID CONN		08/12/2021
130	256	TOUCHID SUPPORT		08/12/2021
131	266	ICT/FCT-1	J414_MLB_C_0.116.0	
132	267	FCT 2	J414_MLB_C_0.116.0	
133	268	PMU AND OTHER TEST POINTS		08/29/2021
134	270	Debug: LEDs, Kobs		02/19/2022
135	271	Debug: Buttons	J414_DTUZYMAN_MLB_S_0.02/15/2022	
136	273	SUPPORT		08/12/2021
137	281	DESENSE CAPS	J414_MIRABEAU_MLB_S_0.11.1 08/12/2021	
138	294	DEBUG: VITAMIN-C	J414_MIRABEAU_MLB_S_0.11.1 02/15/2022	
139	400	POWER ALIASES 1	J414_MIRABEAU_MLB_S_0.11.1 08/30/2021	
140	401	POWER ALIASES 2	J414_MIRABEAU_MLB_S_0.11.1 08/12/2021	
141	402	POWER ALIASES CLVR (S)	CLVR to ref 11/01/2021	
142	403	POWER ALIASES MPMU	T585_REF_PMIC_MAVRICKS_H14_0.36.0	
143	404	POWER ALIASES SPMU	T585_REF_PMIC_MAVRICKS_H14_0.36.0	
144	405	SIGNAL ALIASES - 1 (HIGH SPEED)		08/12/2021
145	406	SIGNAL ALIASES 2		08/12/2021
146	407	SIGNAL ALIASES 3	J414_MIRABEAU_MLB_S_0.11.1 08/12/2021	
147	408	SIGNAL ALIASES 4	J414_MIRABEAU_MLB_S_0.11.1 08/12/2021	
148	410	SIGNAL ALIASES-X2523		08/12/2021
149	501	17.2 RULES		
150	502	17.2 PHYSICAL CSETS		
151	503	17.2 SPACING CSETS, ISO		
152	504	17.2 SPACING CSETS, CLASS-CLASS		
153	600	USBC & NAND BOM OPTION		10/08/2021
154	601	BOM OPTION TABLES-2	J414_MIRABEAU_MLB_S_0.11.1 10/08/2021	
155	602	BOM GROUPS		

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-08012	1	SCHEM,MLB-S,X2523	SCH	CRITICAL	SCH
820-02841	1	PCBF,MLB-S,X2523	PCB	CRITICAL	PCB

DRAWING TITLE			
SCHEM,MLB-S,X2523			
Apple Inc.		DRAWING NUMBER	051-08012
		REVISION	4.0.0
		BRANCH	evt-1
		PAGE	1 OF 700
		SHEET	1 OF 159
NOTICE OF PROPRIETARY INFORMATION: THIS INFORMATION CONTAINS HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC. TO MAINTAIN THIS DOCUMENT IN CONFIDENTIALITY IT IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER OR PUBLISHED IN WHOLE OR PART IN ANY MANNER.			

	8	7	6	5	4	3	2	1
D								
		SOC_H148:5,6,8,10,12,14,16,20,23,25,27,29,31,33,35,37,39,41,42,43						
		WHAMOLA_MP 52,53						
		MAGSAFE_ACE2_20V:54,55						
		ICEMAN:57,58						
		MAVERICKS:76-84,403,404						
		AUSTRINGER:93-95						
		MIRABEAU:101,102,106,118						
		400->402						
		USBC:150-157,159,160,162-164,166-167,169						
C								
		HDMI_COBRA:175-179						
		SDCARD_GL9755:195-198						
		REF_WIRELESS_WILLAMETTE:200-201						
		REF_STORAGE_85E_MARK2 220-229						
		REF_BLC_LUXE:238						
		REF_SKPRAMP_SN012776:246,247						
		REF_IPD:251-254						
B								
		AUSTRINGER:89451 flip overwrite						
		UL1010 and UL111 ALF removed						
A								
	8	7	6	5	4	3	2	1

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	DATE/ TIME	SYNC DATE/TIME
T585	REF_SOC_H148	5,6,8,10,12,14,16,20,23,25,27,29,31,33,35,37,39,41,42,43	0.16.0	S	2022_05_19_14:54:37
T585	REF_SE_BOS	50	0.2.2	S	2022_02_14_16:55:21
T585	REF_CHARGER_WHAMOLA_MP	52,53	0.16.8	S	2022_02_28_15:18:13
T585	REF_MAGSAFE_ACE2_20V	55	0.4.27	S	2022_02_01_11:59:38
T585	REF_VR_ICEMAN	57,58	1.46.0	S	2022_02_28_12:05:17
T585	REF_PMIC_MAVERRICKS_H14	76-84,403,404	0.36.0	S	2022_04_18_13:48:36
T585	REF_VR_AUSTRINGER	93-95	0.34.0	S	2022_05_24_10:43:45
T585	REF_CLVR_MIRABEAU	101,102,106,118	0.39.0	S	2022_06_18_13:41:06
T585	REF_VR_5V_SN621371	122	0.9.0	S	2022_02_03_09:45:59
T585	REF_IMU_SOVEREIGN	144	0.15.0	S	2021_09_24_23:28:56
T585	REF_USBC_LFPA_3PWT_ACE2	166	0.52.3	S	2022_02_22_17:56:43
T585	REF_USBC_VR_L78642_1	158	0.9.0	S	2022_02_02_11:40:19
T585	REF_USBC_VR_TP862180	168	0.8.0	S	2021_12_14_15:15:34
T585	REF_VR_RT13_PORTABLES	159,169	0.13.0	S	2022_04_22_13:20:43
T585	REF_HDMI_COBRA	175-179	0.36.0	S	2021_10_15_12:08:47
T585	REF_SDCARD_GL9755_V2	195-198	0.7.0	S	2022_02_22_17:51:06
T585	REF_WIRELESS_WILLAMETTE	200-201	0.26.0	S	2022_04_18_14:02:40
T585	REF_STORAGE_85E_MARK2	220-229	0.14.0	S	2022_02_03_10:59:35
T585	REF_BLC_LUXE	238	0.34.0	S	2022_04_22_11:26:49
T585	REF_SECDIS_LAS_H14X	242	0.3.0	S	2021_09_25_00:08:29
T585	REF_SECDIS_H14X	243	0.6.0	S	2021_09_25_00:18:54
T585	REF_CODECC_CARLOW	245	1.6.0	S	2021_09_25_00:27:21
T585	REF_SKPRAMP_SN012376	246,247	3.8.0	S	2022_02_15_10:46:21
T585	REF_BLC_BEN_XPD_ONLY	250	0.7.0	S	2022_02_03_09:07:36
T585	REF_IPD	251-254	0.30.0	S	2022_05_04_19:11:56
T585	REF_DEBUG_STUFF	270,271,294	0.3.0	S	2022_02_15_11:26:26
J414.DYDEMANN	MLB_S	19	0.61.1	S	2021_12_09_13:12:19
J414	MLB_C	3	2.23.0	S	2022_02_03_10:37:57
J414.HKURRATI	MLB_S	135-139	1.14.2	S	2022_02_21_12:33:37
J414.JERRYLIU	MLB_S	234	0.46.1	S	2021_11_08_20:34:41

SYNC MASTER		PAGE TITLE		PAGE: 0000000/00000001	
REFERENCE DESIGN TABLE					
 Apple Inc.	DRAWING NUMBER		PAGE		
	051-08012		D		
	REVISION		4.0.0		
NOTICE OF PROPRIETARY PROPERTY:		ISSUANCE		evt-1	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE REVISION AGREES TO THE FOLLOWING:		PAGE		2 OF 700	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET		2 OF 159	
I NOT TO REPRODUCE OR COPY IT					
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART					
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE					
I NOT TO REPRODUCE OR COPY IT					
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART					

MAGSAFE BOSS

BS0450
2.7X1.8R-1.4ID-1.7H-SM
860-01714BS0451
2.7X1.8R-1.4ID-1.7H-SM
860-01714

L USBC BOSS

BS04F0
2.7X1.8R-1.4ID-1.7H-SM
860-01714BS04F1
2.7X1.8R-1.4ID-1.7H-SM
860-01714BS04F2
2.7X1.8R-1.4ID-1.7H-SM
860-01714

R USBC BOSS

BS04G0
2.7X1.8R-1.4ID-1.7H-SM
860-01714BS04G1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

ANTENNA BOSS

BS04L0
2.7X1.8R-1.4ID-1.7H-SM
860-01714BS04L1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

DISP, CAM BOSS

BS04P0 860-01924
BOSS-3.2OD1.4D-1.7H-SMBS04P1 860-01924
BOSS-3.2OD1.4D-1.7H-SM

TRACKPAD BOSS

BS04T0
3.4OD1.75ID-2.0IH-SM
860-01805BS04T1
3.4OD1.75ID-2.0IH-SM
860-01805

BKLT BOSS

BS04P2 860-01924
BOSS-3.2OD1.4D-1.7H-SMBS04P3 860-01924
BOSS-3.2OD1.4D-1.7H-SM

LAS BOSS

BS04R0
2.7X1.8R-1.4ID-1.7H-SM
860-01714BS04R1
2.7X1.8R-1.4ID-1.7H-SM
860-01714

AUDIO JACK BOSS

BS04R4
2.7X1.8R-1.4ID-1.7H-SM
860-01714BS04R5
2.7X1.8R-1.4ID-1.7H-SM
860-01714

TOUCHID BOSS

BS04T2 860-01936
2.7X1.8R-1.34H-SMBS04T3 860-01936
2.7X1.8R-1.34H-SMPLATED HOLES NEAR SOC
TH0400/1/3 remove 08/26/2021

STIFFENER

APN in BOM TABLE

VIPER SHIELD FENCE

SH0476
FENCE-MLB-BTN-NAND-X940

SH0477
FENCE-TITAN-RIDGE-X940

TOP-SIDE BUMPERS

860-01819 (was 860-01209)
(was 860-01742)BM0400
2.8OD1.2ID-1.703H-SM
860-01819BM0403
2.8OD1.2ID-1.703H-SMBM0405
2.8OD1.2ID-1.703H-SMBM0408
2.8OD1.2ID-1.703H-SMBM0404
2.8OD1.2ID-1.703H-SMBM0406
2.8OD1.2ID-1.703H-SMBM0410
2.8OD1.2ID-1.703H-SMBM0402
2.8OD1.2ID-1.703H-SMBM0407
2.8OD1.2ID-1.703H-SMBM0413
2.8OD1.2ID-1.703H-SM

BOTTOM-SIDE BUMPERS

BM0430
2.8OD1.2ID-3.416H-SM
860-01820BM0434
2.8OD1.2ID-3.416H-SM
860-01820BM0437
2.8OD1.2ID-3.416H-SM
860-01820BM0435
2.8OD1.2ID-3.416H-SM
860-01820

SHIELD FRAMES

SH0470
FENCE-TITAN-RIDGE-X940
OMIT TABLESH0471
FENCE-MLB-BTN-NAND-X940
OMIT TABLESH0473
FENCE-MLB-BTN-NAND-X940
OMIT TABLESH0474
FENCE-TITAN-RIDGE-X940
OMIT TABLESH0472
FENCE-TITAN-RIDGE-X940
OMIT TABLESH0475
FENCE-MLB-BTN-NAND-X940
OMIT TABLE

ANTENNA CLIPS

PLATED SLOTS NEAR SOC

CL0400 860-01841
BOSS-2.9X4.7-2.1H-SMShield CAN Alignment Slots 8X
- 998-04440 (1.2mm X 0.4mm)SH0445
SL-1.2X0.4-1.5X0.7
870-12170SH0449
SL-1.2X0.4-1.5X0.7SH0453
SL-1.2X0.4-1.5X0.7SH0457
SL-1.2X0.4-1.5X0.7SH0446
SL-1.2X0.4-1.5X0.7SH0450
SL-1.2X0.4-1.5X0.7SH0454
SL-1.2X0.4-1.5X0.7SH0458
SL-1.2X0.4-1.5X0.7SH0447
SL-1.2X0.4-1.5X0.7SH0451
SL-1.2X0.4-1.5X0.7SH0455
SL-1.2X0.4-1.5X0.7SH0459
SL-1.2X0.4-1.5X0.7SH0448
SL-1.2X0.4-1.5X0.7SH0452
SL-1.2X0.4-1.5X0.7SH0456
SL-1.2X0.4-1.5X0.7SH0460
SL-1.2X0.4-1.5X0.7

POGO 870-12170

PG0400
POGO-2.3OD-4.33H-SM
870-12170PG0404
POGO-2.3OD-4.33H-SMPG0408
POGO-2.3OD-4.33H-SMPG0401
POGO-2.3OD-4.33H-SMPG0405
POGO-2.3OD-4.33H-SMPG0409
POGO-2.3OD-4.33H-SMPG0402
POGO-2.3OD-4.33H-SMPG0406
POGO-2.3OD-4.33H-SMPG0410
POGO-2.3OD-4.33H-SMPG0403
POGO-2.3OD-4.33H-SMPG0407
POGO-2.3OD-4.33H-SMPG0411
POGO-2.3OD-4.33H-SM

STIFFENER

806-29576
STIFFENER-MLB-LC-X1930
OMIT TABLE806-29573
STIFFENER-MLB-LC-X1930
OMIT TABLE806-29575
STIFFENER-MLB-LC-X1930
OMIT TABLE806-29572
STIFFENER-MLB-LC-X1930
OMIT TABLE806-29574
STIFFENER-MLB-LC-X1930
OMIT TABLE806-29572
STIFFENER-MLB-LC-X1930
OMIT TABLE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-35724	1	SHIELD,FENCE,BRIDGE,RT,UPDATE,X2465	SH0470	CRITICAL	
806-34681	1	SHIELD,FENCE,BRIDGE,LEFT,X1930	SH0471	CRITICAL	
806-34683	1	SHIELD,FENCE,VIPER,RIGHT,X1930	SH0472	CRITICAL	
806-34682	1	SHIELD,FENCE,VIPER,LEFT,X2465	SH0473	CRITICAL	
806-34684	1	SHIELD,FENCE,RIGHT,X2465	SH0474	CRITICAL	
806-34685	1	SHIELD,FENCE,MAVERICK,X2465	SH0475	CRITICAL	
806-36029	1	FENCE,VIPER,TOP,LEFT,X2465	SH0476	CRITICAL	
806-36030	1	FENCE,VIPER,TOP,RIGHT,X2465	SH0477	CRITICAL	
806-29576	1	STIFFENER,CORNER,LT,UP,MLB,X1930	ST0410	CRITICAL	
806-29575	1	STIFFENER,CORNER,RT,UP,MLB,X1930	ST0411	CRITICAL	
806-29574	1	STIFFENER,LEFT,MID,MLB,X1930	ST0412	CRITICAL	
806-29573	1	STIFFENER,RT,MID,MLB,X1930	ST0413	CRITICAL	
806-29572	2	STIFFENER,MLB,CORNER,LOWER,X1930	ST0414,ST0415	CRITICAL	
806-36016	1	STIFFENER,CHARLES,DIMPLES,0.30,30X,30X,X1930	STFNR	CRITICAL	STFNR

PD PARTS			
 Apple Inc.	PROCESSING NUMBER	051-08012	PAGE D
	REVISION	4.0.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE INFORMATION AGREED TO BE KEPT 1 TO MAINTAIN THIS DOCUMENT IN CONFERENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED	STAGE	evt-1	
	PAGE	4 OF 700	
	FILE	3 OF 159	

BOM_COST_GROUP=MECHANICALS

D

C

B

A

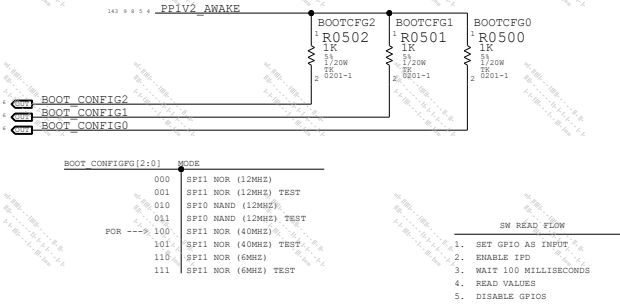
D

C

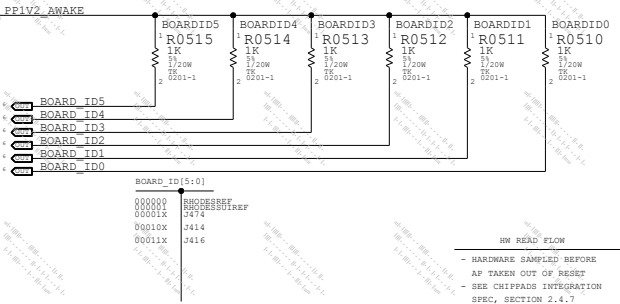
B

A

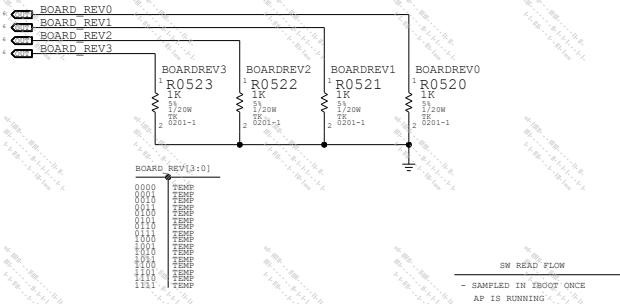
BOOT CONFIG



BOARD ID

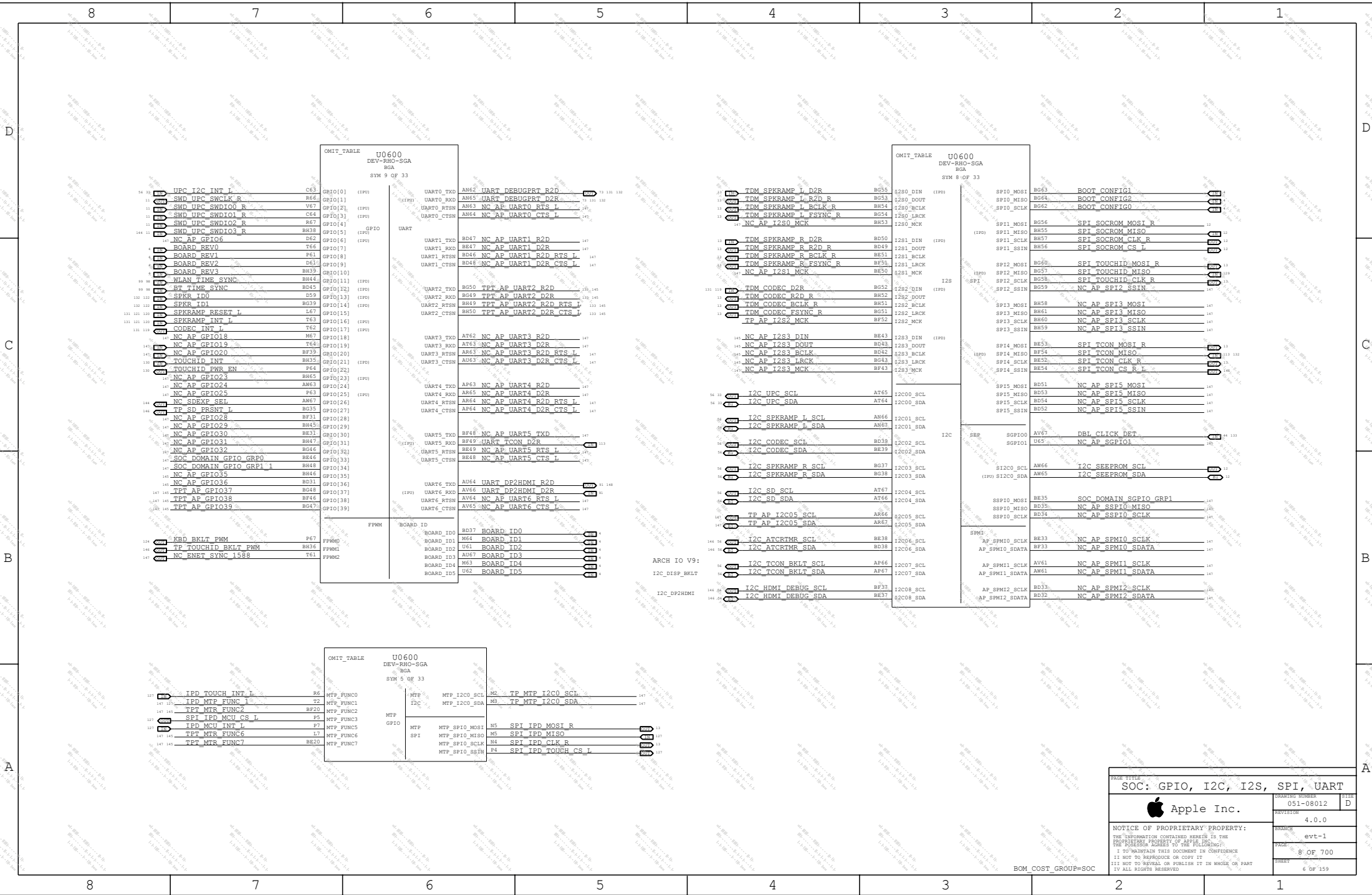


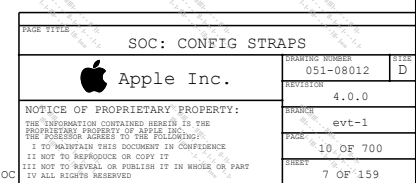
BOARD REV

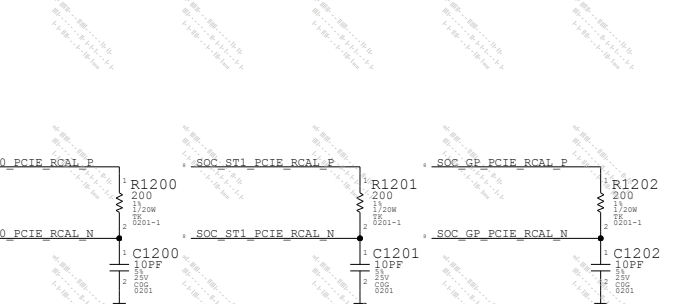
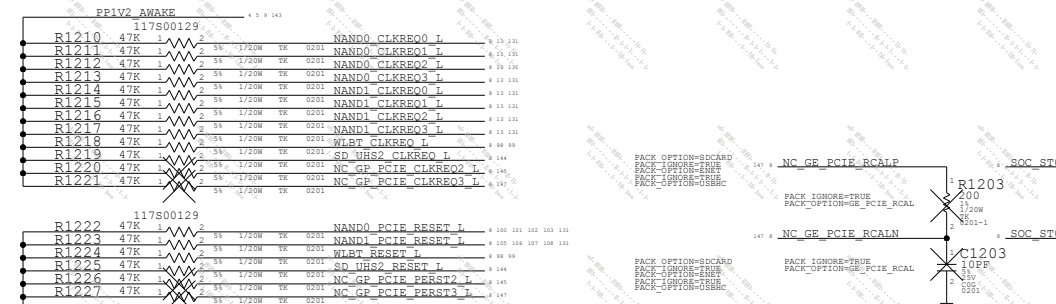
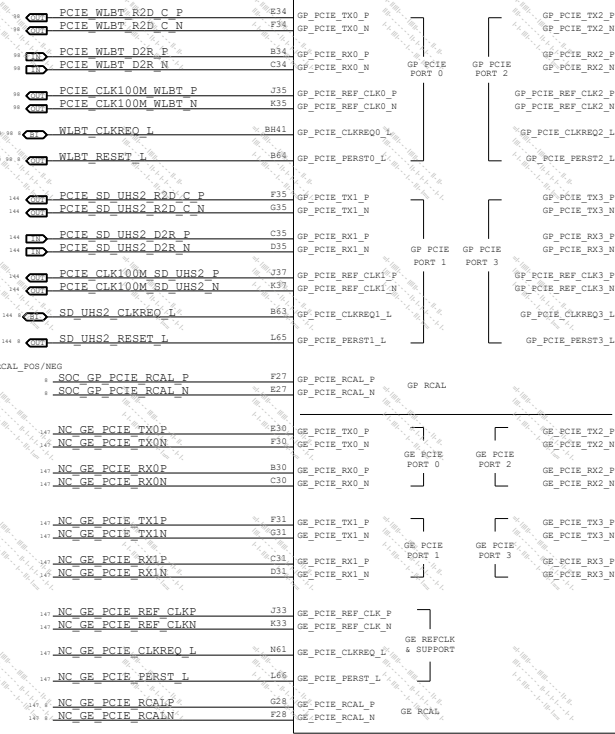
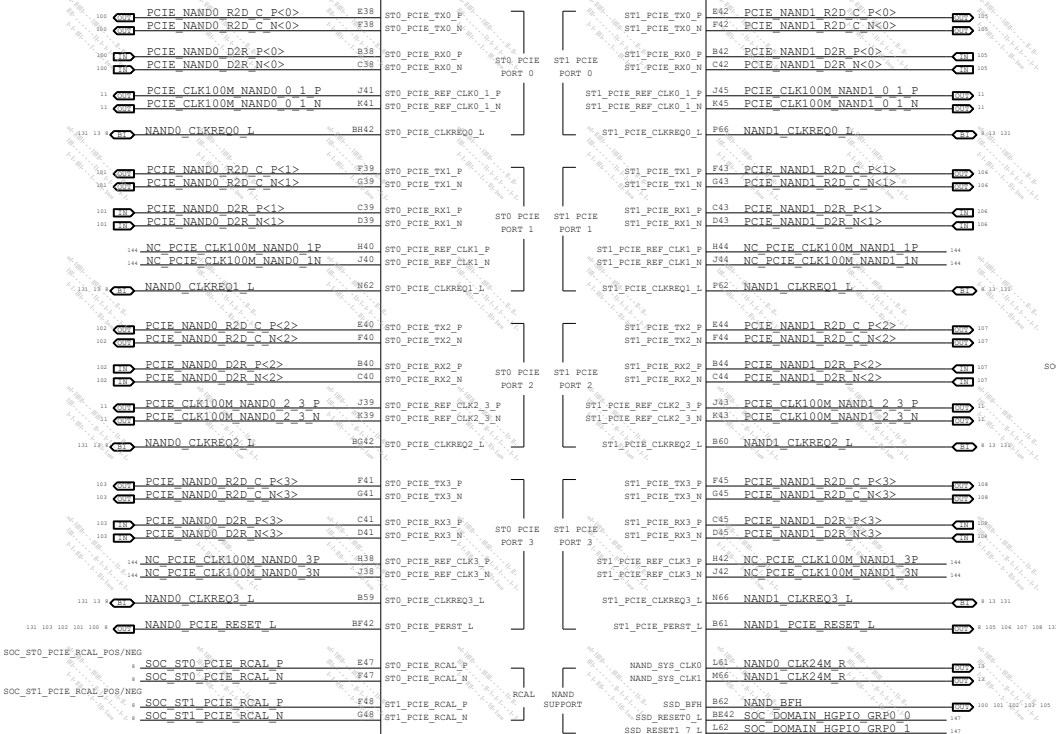


BOM_COST_GROUP=SOC

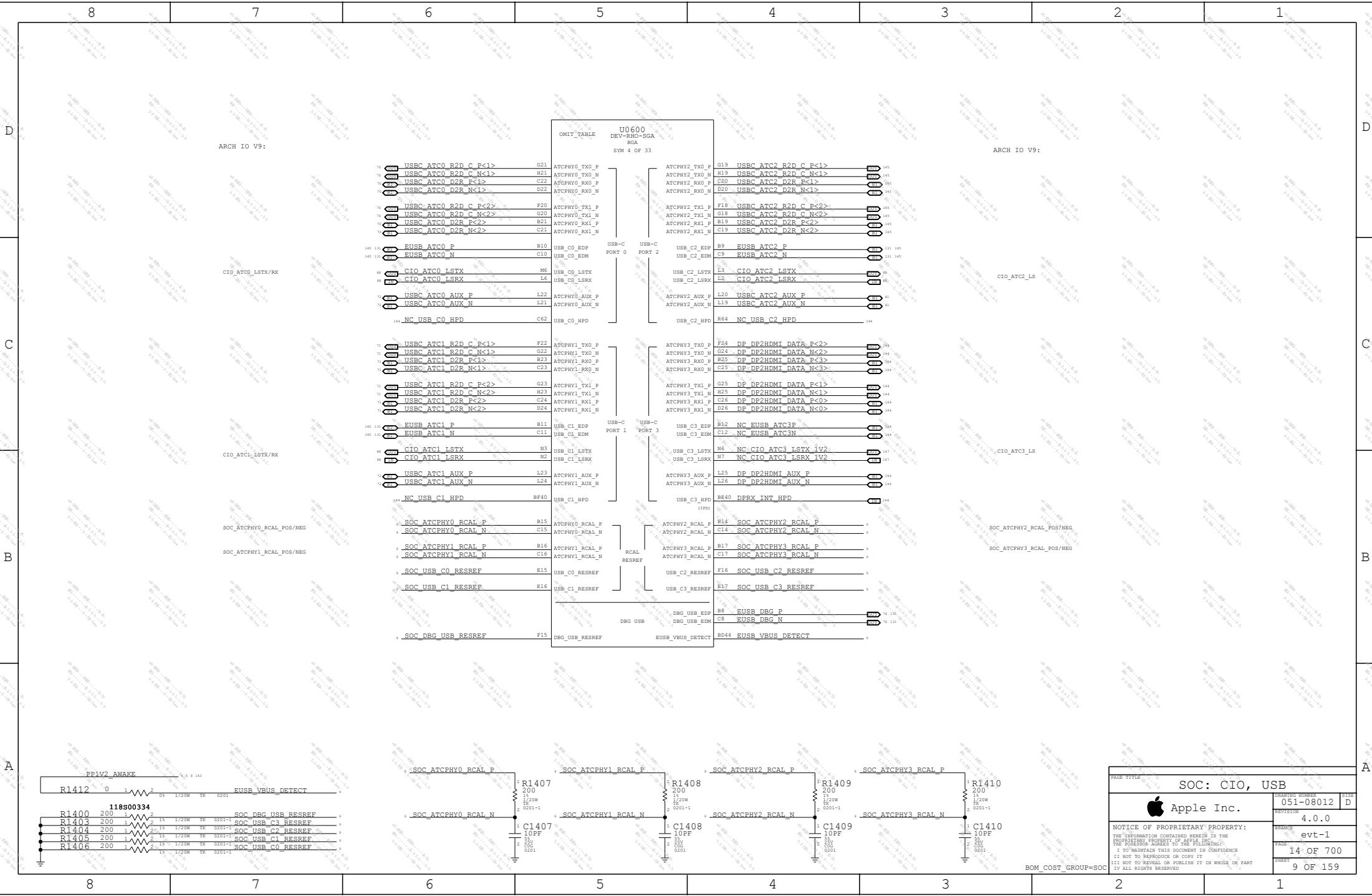
PAGE TITLE		
SOC: CONFIG STRAPS		
 Apple Inc.	REVISION	051-08012
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE EXPRESS WRITTEN PERMISSION OF APPLE INC. I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I WILL NOT REVEAL OR PUBLISH IT IN WHOLE OR PART IN ANY MANNER.	STAGE	evt-1
	PAGE	5 OF 700
	PAGE	4 OF 159

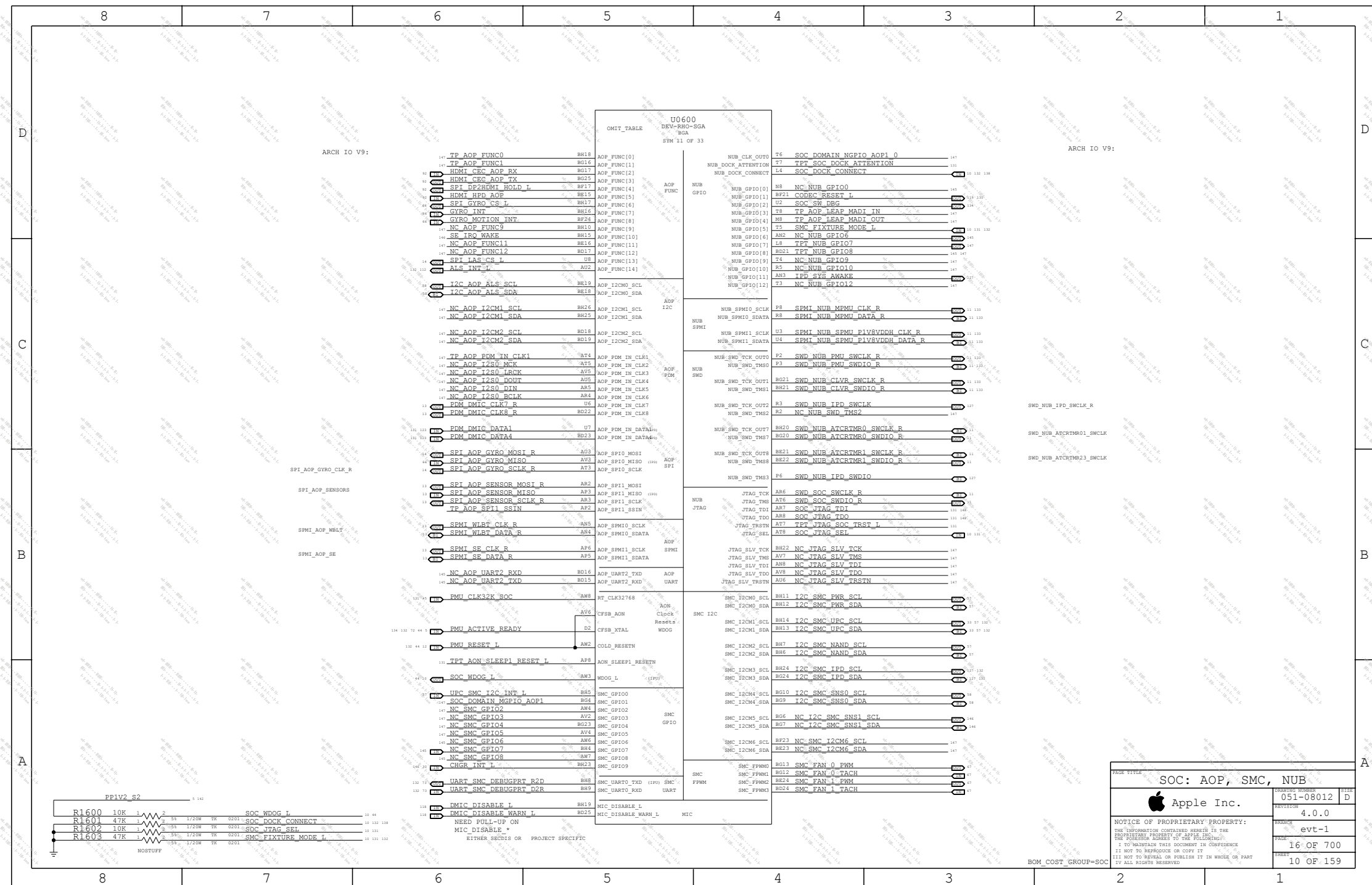






PAGE TITLE			
SOC: PCIE			
 Apple Inc.	DRAWING NUMBER	051-08012	
	REVISION	4.0.0	
	EXPLODED	evt-1	
	PAGE	12. OF 700	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE RECIPIENT AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I TO NOT TO REVEAL OR PUBLISH IT IN WRITTEN OR PART I ALL RIGHTS RESERVED			
SHEET		8 OF 159	

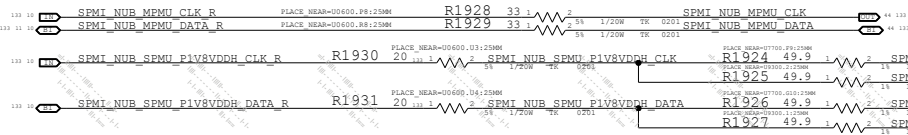
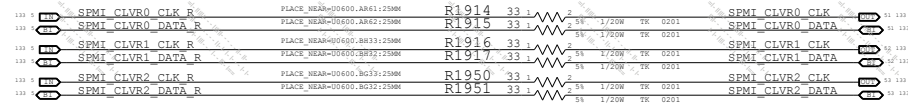




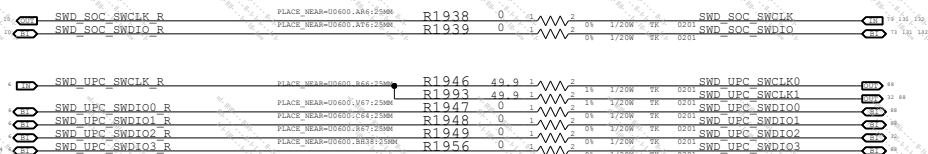
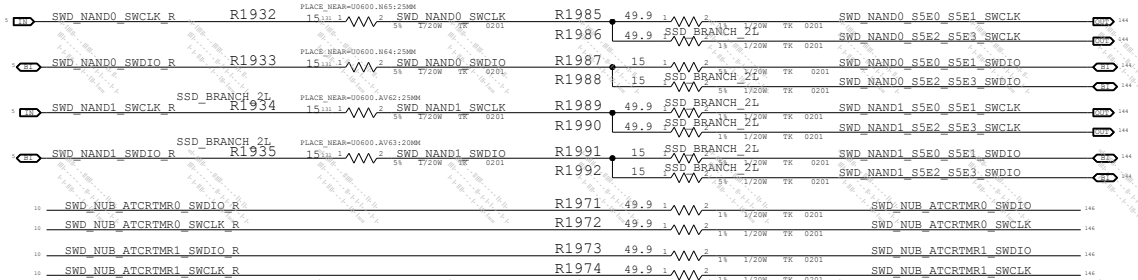
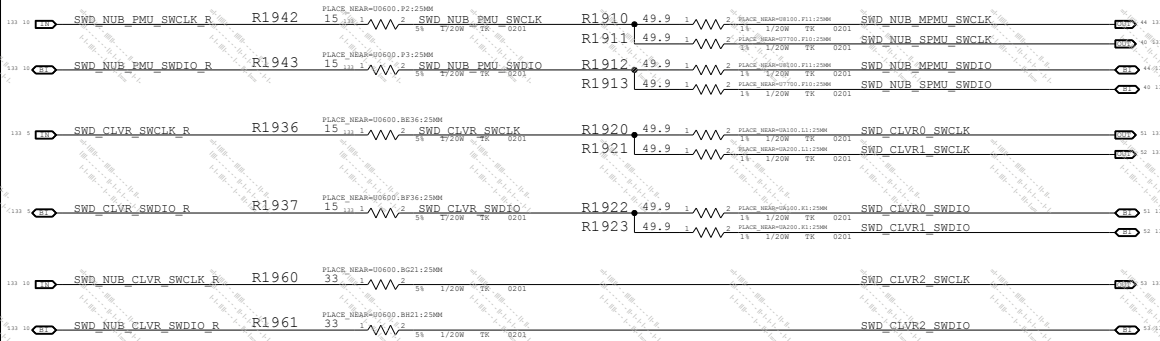
IN PROGRESS

SPMI PMU SERIES RESISTORS

TODO: check resistor values with SI sims



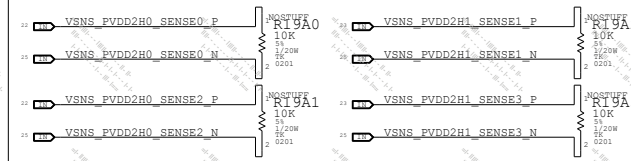
SWD SERIES RESISTORS



VDD/VSS SENSE BREAKOUT PADS

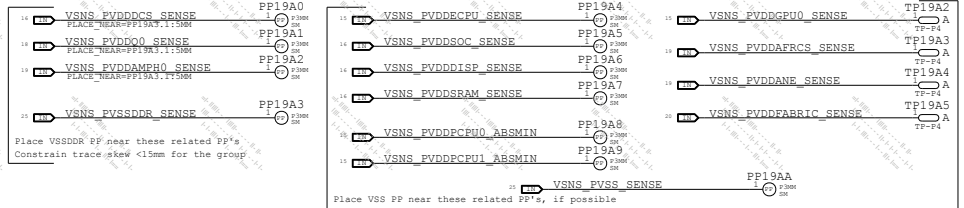
All SOC/DRAM VSSNS traces to be 50ohm SE-impedance

Non-CLVR SENSE points are only for debug/characterization access
Non-CLVR diff SENSE use resistor pads. These will never be STUFF'd:



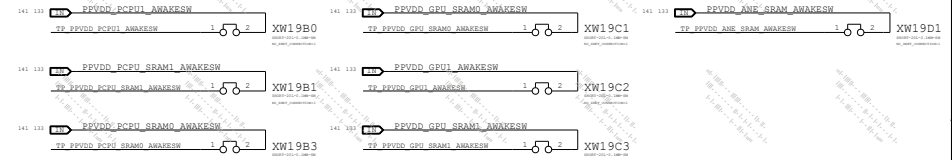
CLVR rail SENSE points are used in Factory in place of fixture probe access on PP* net, so they require HWTE TPs:

P/N pairs do not require diff impedance control, But should be routed as a pair for noise immunity

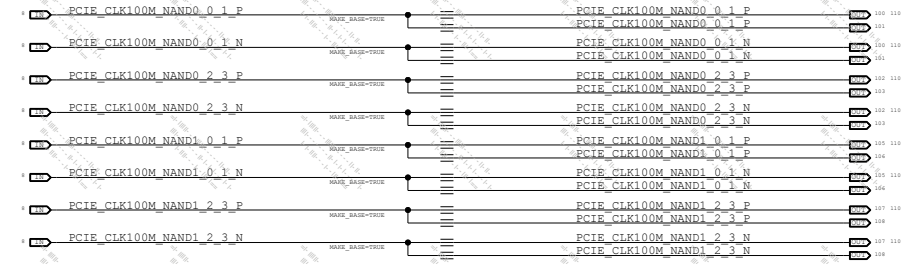


HWTE access to CLVR outputs

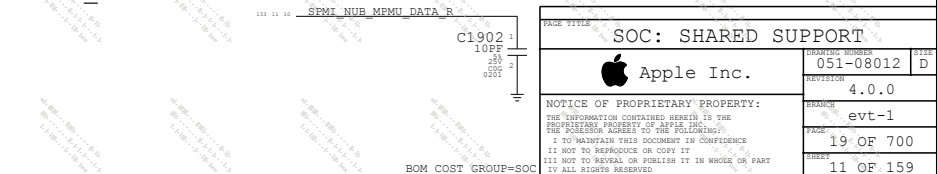
TP19A* SENSE TPs can be used in place of output nets. Below are the CLVR outputs that don't have a SENSE TP
Place XWS under CLVRs, to breakout to HWTE-accessible test vias
TP_PVDD nets require special spacing constraints to all nets except GND



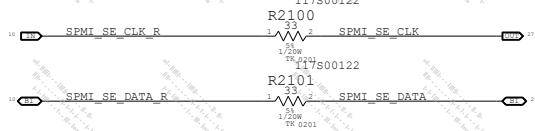
NAND PCIE CLK BRANCH RESISTORS



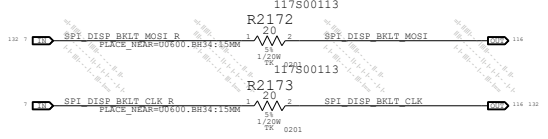
SPMI_NUB DAMPING FILTERS



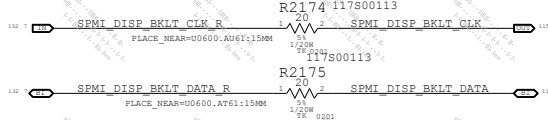
SGA SPMI SE SOURCE TERMINATIONS



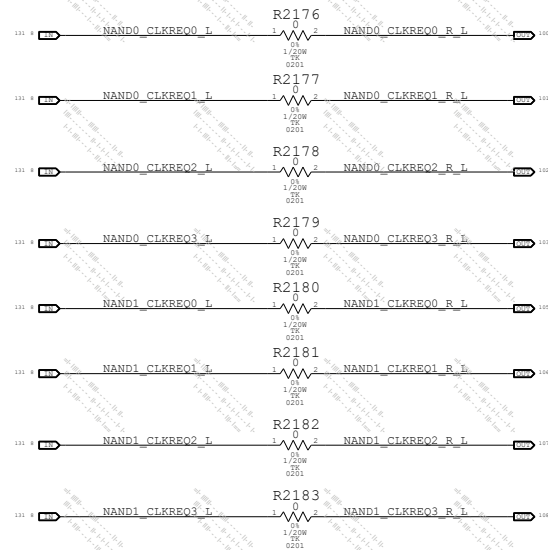
SGA SPI BKLK SOURCE TERMINATIONS



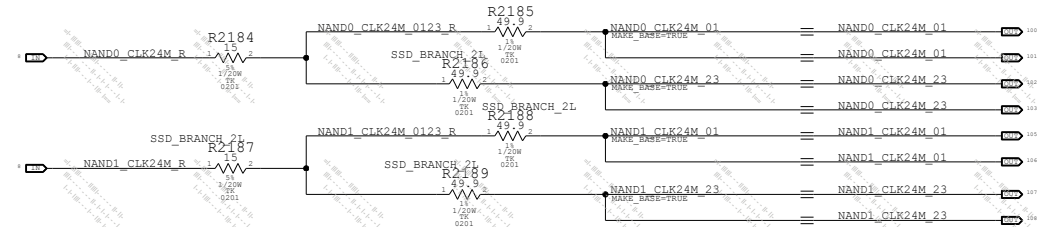
LUXE SPMI SOURCE TERMINATIONS



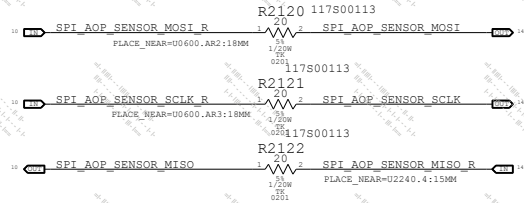
NAND CLKREQ SERIES RESISTORS



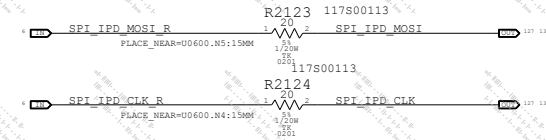
SSD 24M CLOCK TERMINATIONS



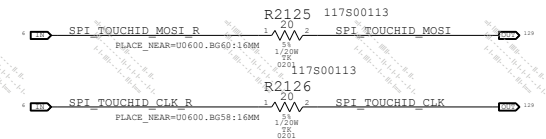
SGA SPI SENSOR SOURCE TERMINATIONS



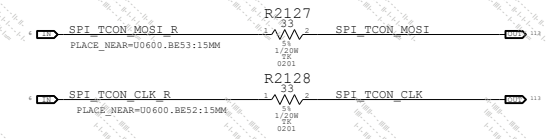
SGA SPI IPD SOURCE TERMINATIONS



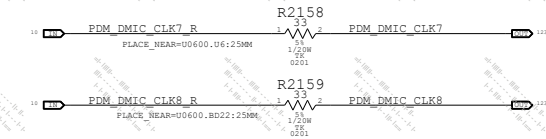
SGA SPI TOUCHID SOURCE TERMINATIONS



SGA SPI TCON SOURCE TERMINATIONS



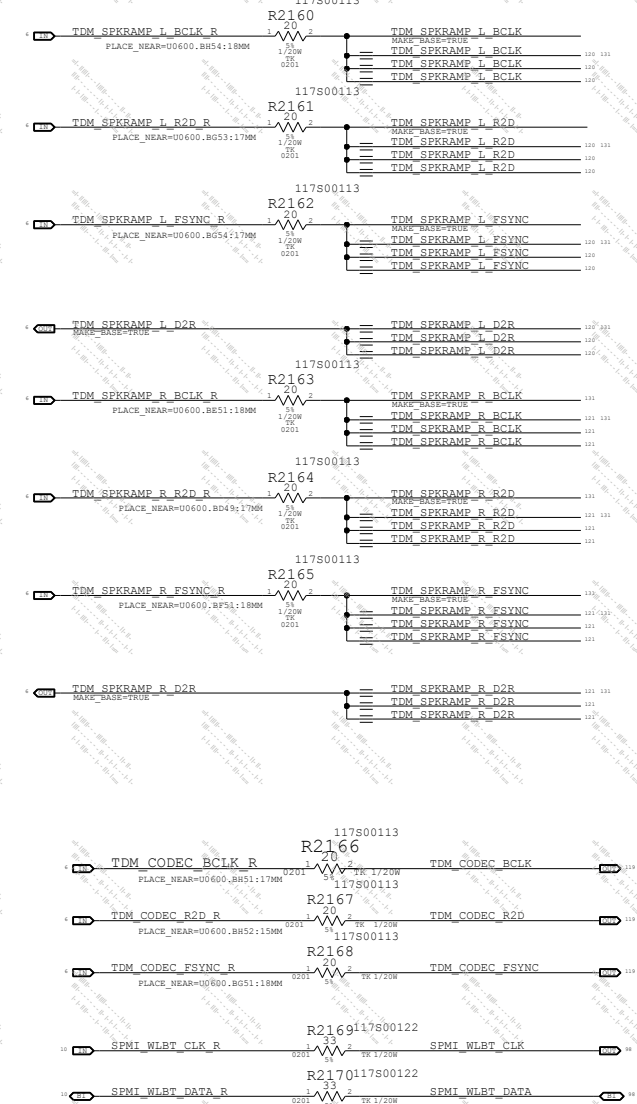
DMIC CLK SOURCE TERMINATIONS



TCON CS



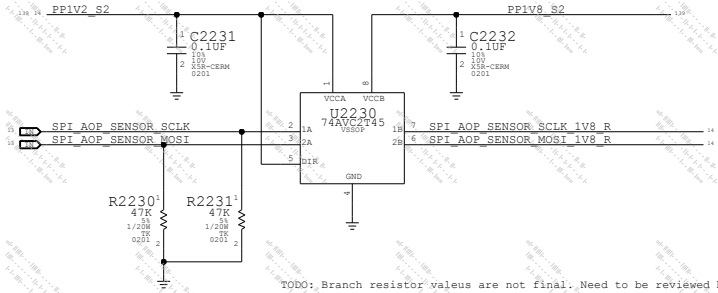
SGA TDM SOURCE TERMINATIONS



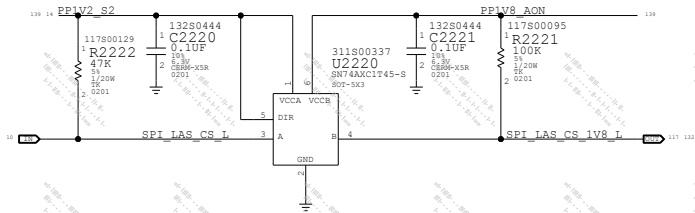
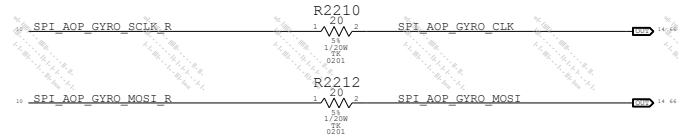
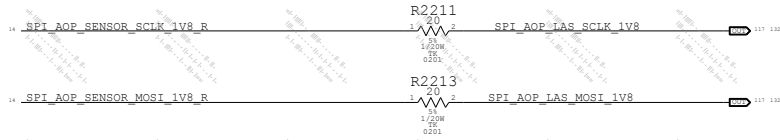
PAGE TITLE			
PROJECT SUPPORT (1/2)			
Apple Inc.	REVISION	051-08012	D
	REVISION	4.0.0	
NOTICE OF PROPRIETARY PROPERTY:	REVISION	evt-1	
	REVISION	21 OF 700	
BOM_COST_GROUP=SOC			13 OF 159

SPI AOP Sensor LS and Branch Resistors

TODO: Reference designators need to be updated once layout has imported latest netlist



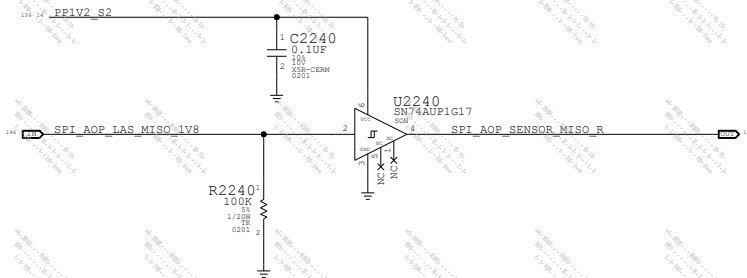
DISPLAY BACKLIGHT



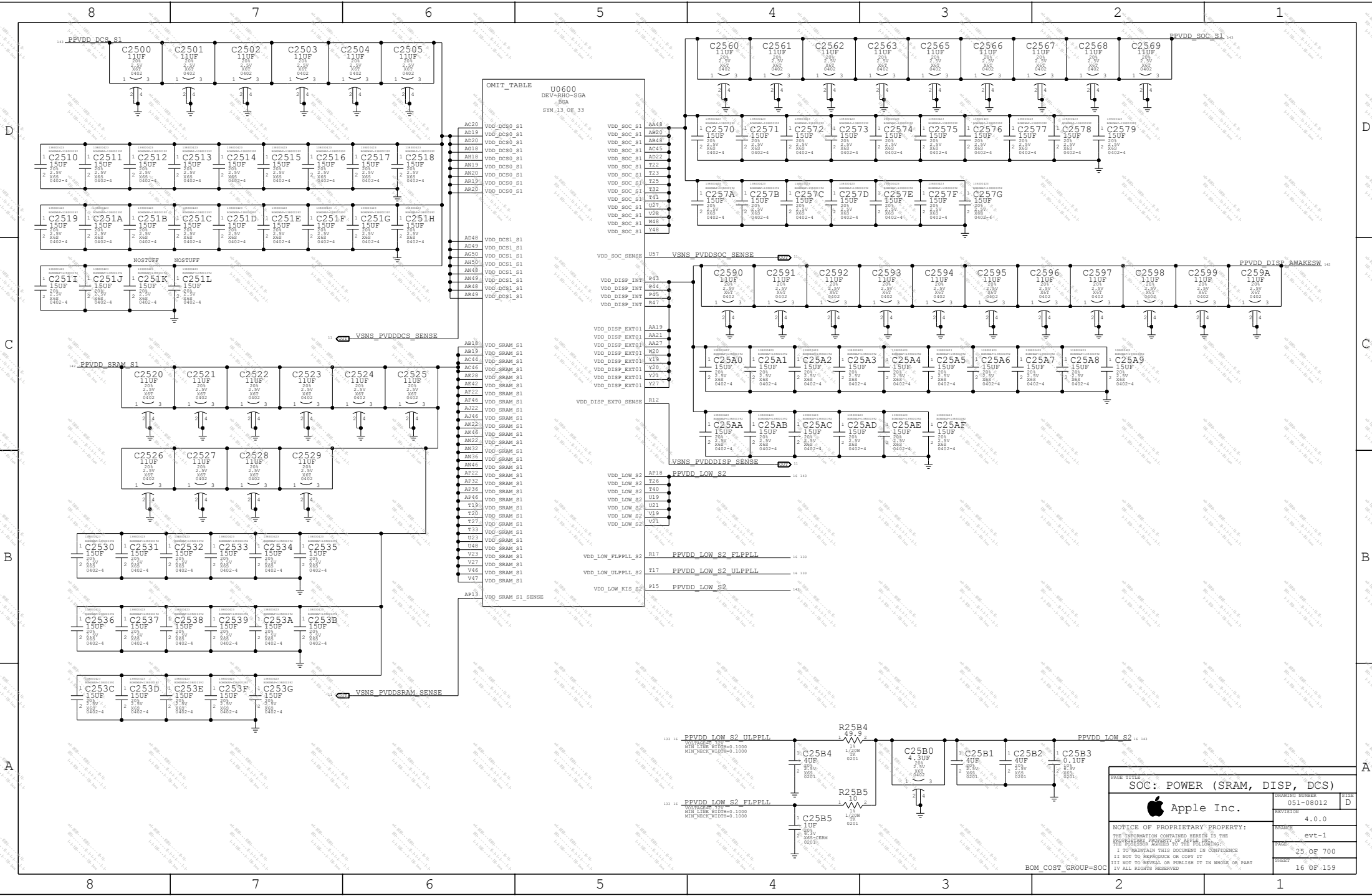
rdar://86287477
(J414x Plx missing PD for AOP_SPI0_MOSI and AOP_SPI0_SCLK)



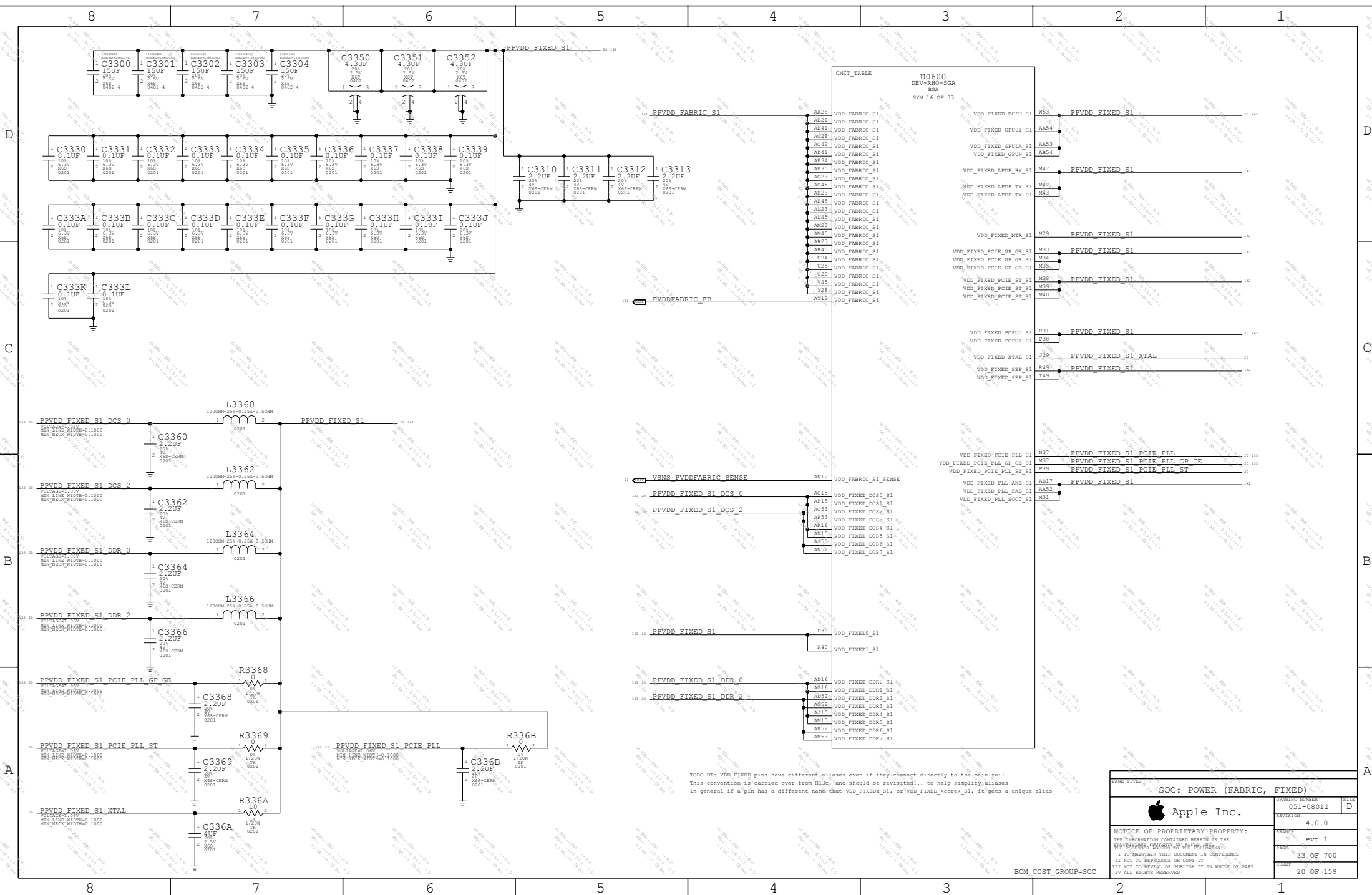
SPI LEVEL TRANSLATION

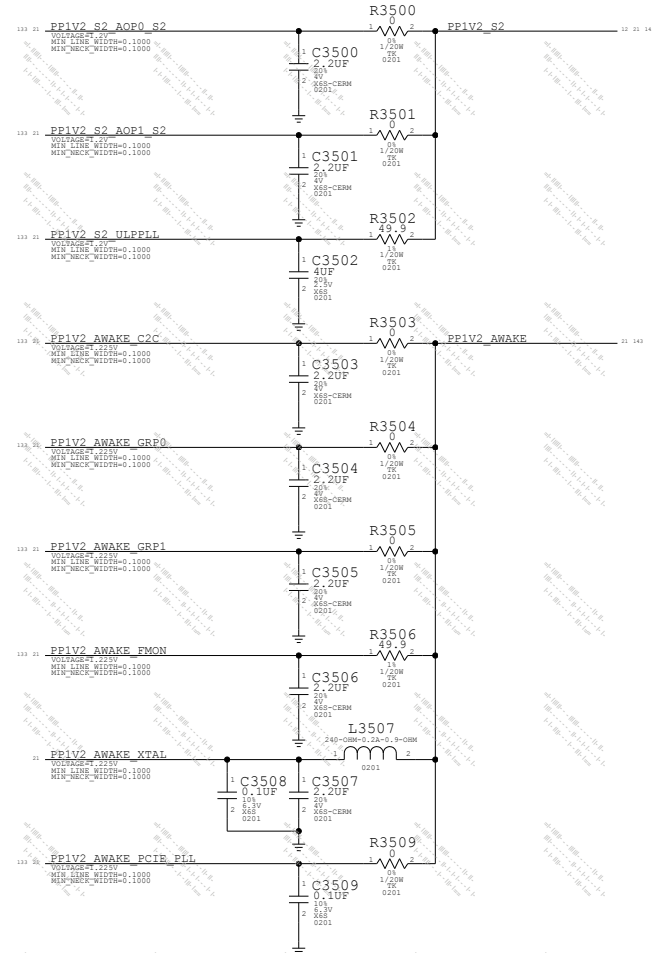
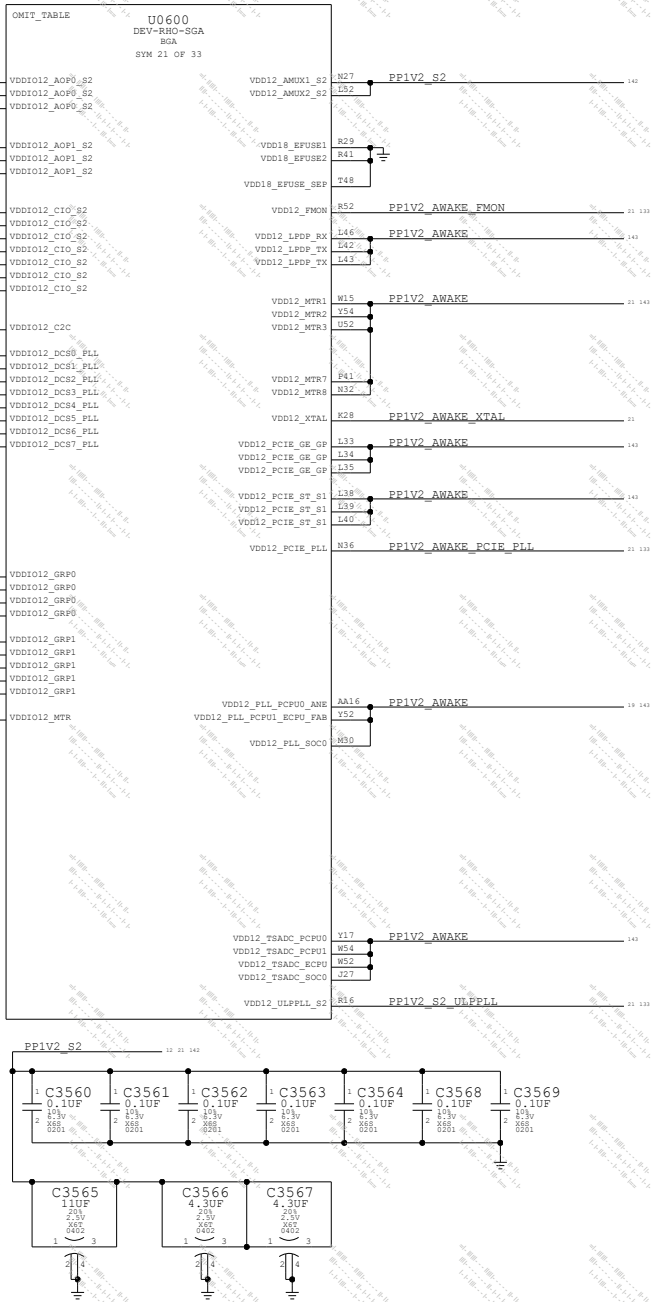
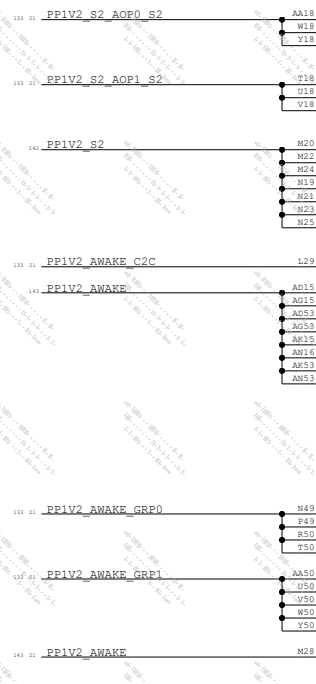
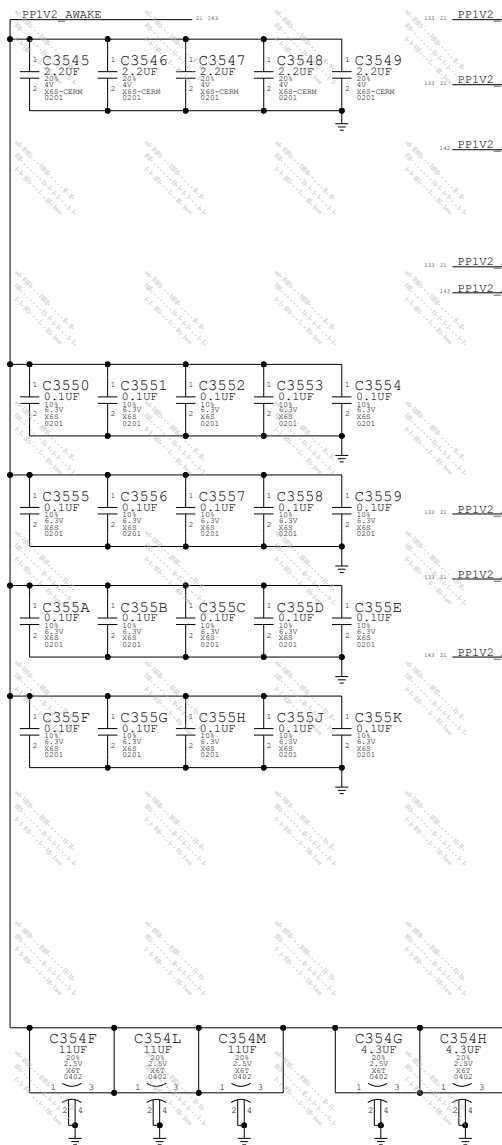


PAGE TITLE		
PROJECT SUPPORT (2/2)		
Apple Inc.	051-08012	PLATE D
	4.0.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. ALL RIGHTS RESERVED. NO PART OF THIS DOCUMENT SHALL BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT PERMISSION IN WRITING FROM APPLE INC.	evt-1	
	22 OF 700	
BOM_COST_GROUP=SOC		14 OF 159



PAGE TITLE			
SOC: POWER (SRAM, DISP, DCS)			
	REVISION	051-08012	REV D
	REVISION	4.0.0	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE EXPRESS WRITTEN PERMISSION OF APPLE INC.			
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
2. NOT TO REPRODUCE OR COPY IT			
3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
4. ALL RIGHTS RESERVED			
BOM_COST_GROUP=SOC			25 OF 700
			16 OF 159





PAGE TITLE		DRAWING NUMBER		SIZE	
SOC: POWER. (VDDIO)		051-08012		D	
 Apple Inc.		REVISION			
		4.0.0			
		BRANCH		ewt-1	
NOTICE OF PROPRIETARY PROPERTY:		PAGE		35 OF 700	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE ADDRESSEE AGREES TO THE FOLLOWING: 1. TO MAINTAIN THEIR OWN CONFIDENTIALITY 2. NOT TO REPRODUCE OR COPY IT 3. NOT TO DISSEMINATE OR PUBLISH IT IN WHOLE OR PART 4. ALL RIGHTS RESERVED		SHEET		21 OF 159	

BOM COST GROUP=SOC

D

D

C

B

A

C

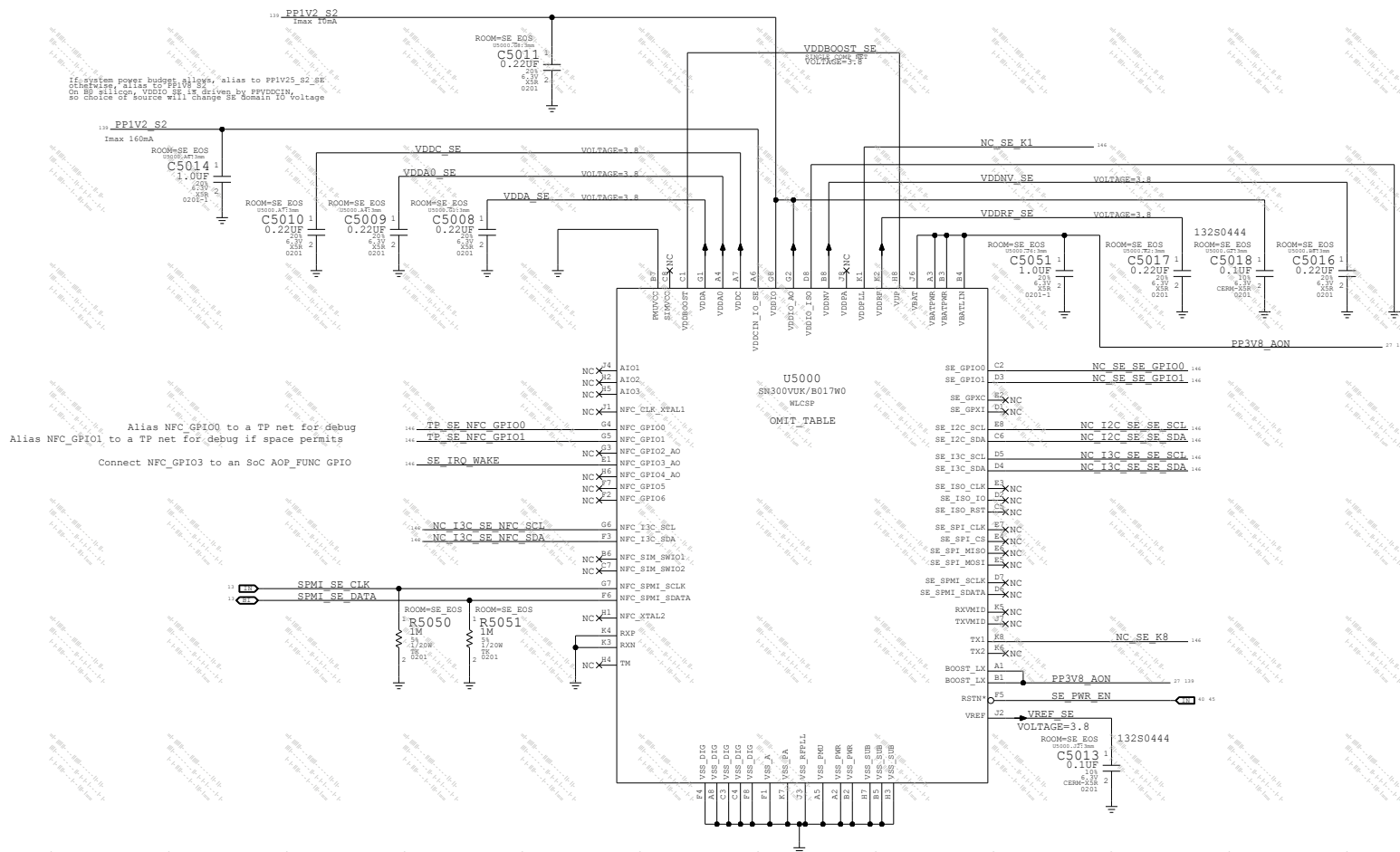
B

A

PAGE TITLE		SOC: GND-3	
 Apple Inc.	DRAWING NUMBER 051-08012	SHEET D	
	PREVISION 4.0.0		
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS TO MAINTAIN THIS DOCUMENT IN CONFIDENCE IT IS NOT TO REPRODUCE OR COPY IT IT IS NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		BRANCH evt-1	PAGE 43 OF 700
OC		SHEETS 26 OF 159	

BOM COST GROUP=SOC

Eos - Secure Element



SE and NFC GPIO, I2C, and I3C are not used on the architectural roadmap as of 9/15/21 and should be NC'd on all form factor designs, with the exception of NFC_GPIO1/2/3 per inline notes

Support for Eos A1 Silicon has been removed from the reference design following V0.1.0

<rdar://problem/59254645> [SN300V] Data Sheet
<rdar://problem/71610778> [SN300V] Wired Mode SE Only Reference Design Material

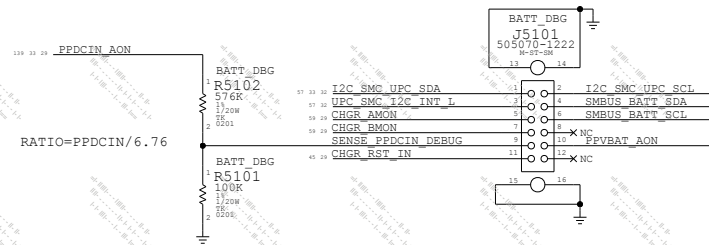
BOM COST GROUP=SECURE ELEMENT

PAGE TITLE		DATE RECORDED	FILE
Secure Element		051-08012	D
 Apple Inc.		REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRAND	evt-1
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.		DATE	50 OF 700
IT IS NOT TO REVEAL OR FURNISH IT IN WHOLE OR PART TO ANY OTHER PERSON OR ENTITY.		TIME	27 OF 159

Battery Sub-System Debug Connector
ARKANOID CONN

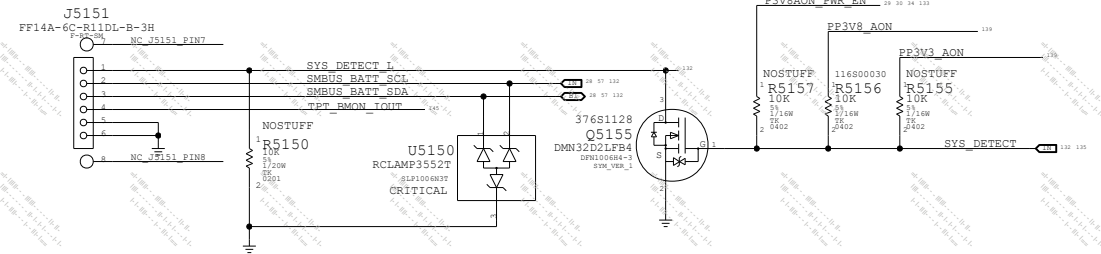
BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-04146	1	PCBA, FLEX, BMU-POWER, X1703	J5150	CRITICAL	



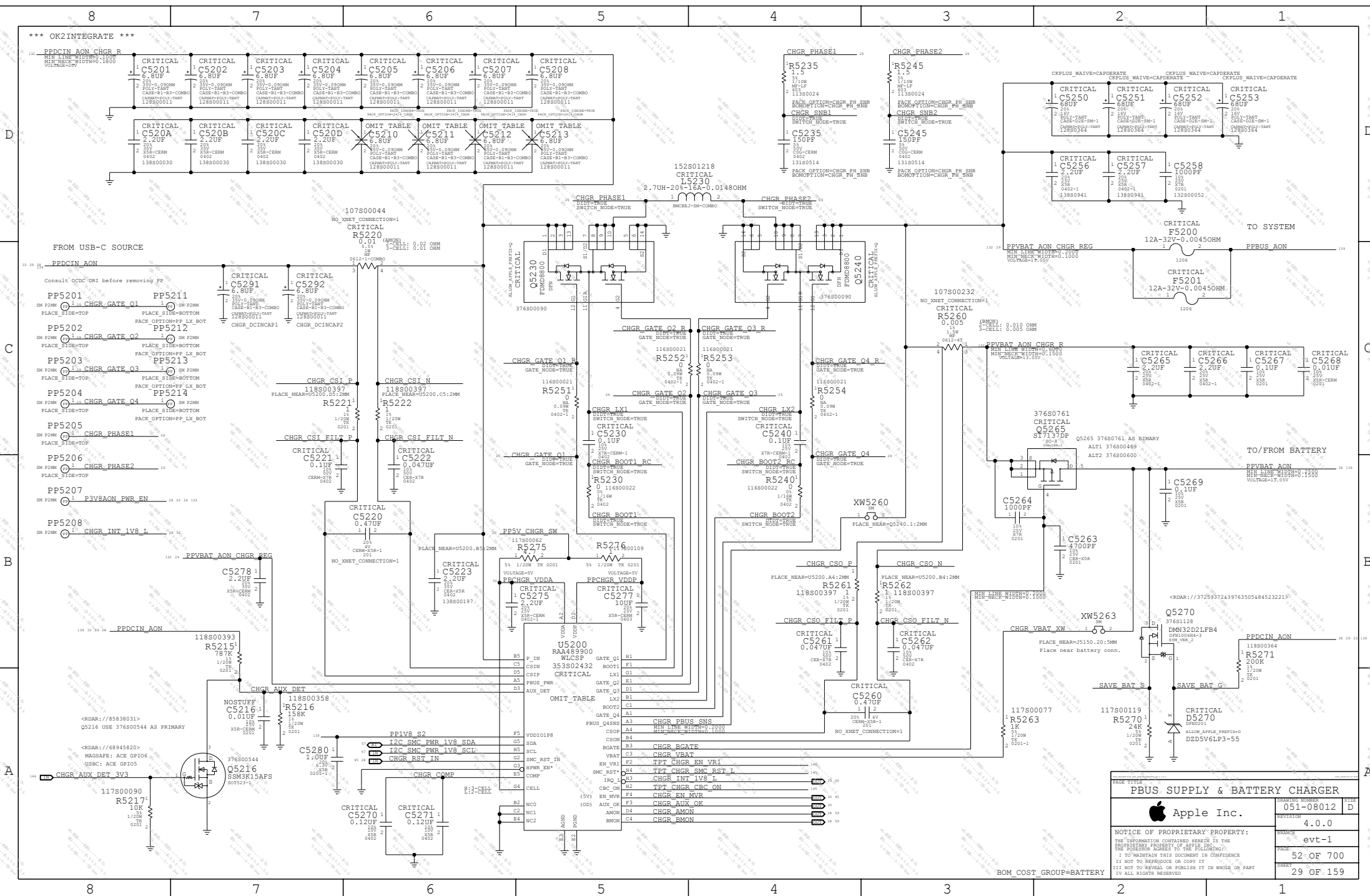
ARKANOID	MLB Connector / Signals	Salese
J0301 - 1	6 SMBUS_BATT_SCL (= I2C_SMC_PWR_SCL)	0
J0301 - 3	4 SMBUS_BATT_SDA (= I2C_SMC_PWR_SDA)	1
J0301 - 5	2 I2C_SMC_UPC_SCL	2
J0301 - 7	1 I2C_SMC_UPC_SDA	3
J0302 - 1	3 UP_CSMC_I2C_INT_L	4
J0302 - 3	5 CHGR_AMON	5
J0302 - 5	7 CHGR_BMON	6
J0302 - 7	9 1 / 6.76 * PPDCIN_AON	7
J0303 - 1	11 CHGR_RST_IN	8
J0303 - 3	12 -	9
J0303 - 5	10 PPVBAT_AON	10
J0303 - 7	8 -	11

APN:518S0818



BATTERY CONN	
Apple Inc.	051-08012
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. IT IS TO BE KEPT CONFIDENTIAL AND NOT TO BE REPRODUCED OR COPIED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM.	4.0.0
51 OF 700	28 OF 159

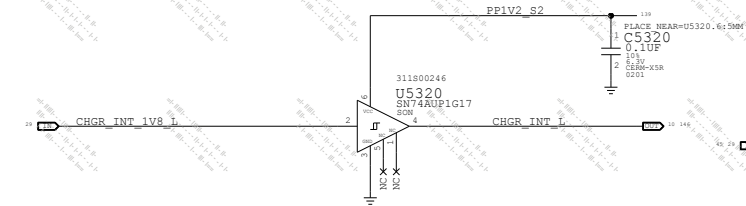
BOM_COST_GROUP=BATTERY



SMBUS_CHGR_IV8 [SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

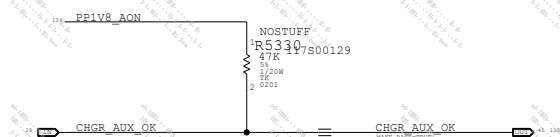
CHGR_INT_L Level Translation

IRQ_L IS PUSH FULL OUTPUT



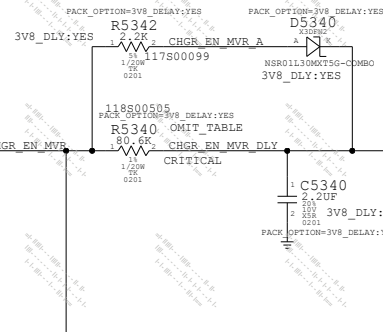
CHGR AUX OK Pull Up

PULL UP TO MPMU LDO9, OR RELY ON MPMU INTERNAL PULL UP.

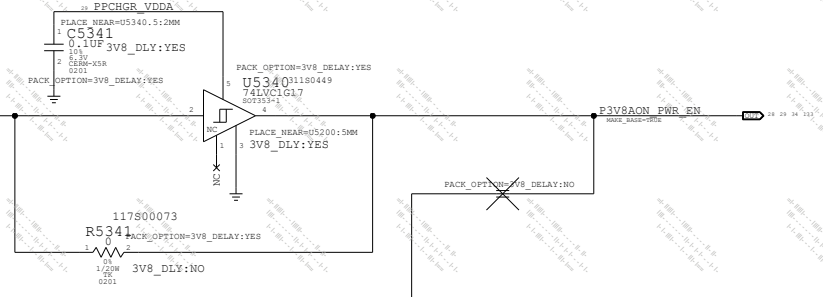


DELAY FOR 3.8V VR ENABLE

R5340 and C5340 updated per rdar://62686034
RDAR://84281699

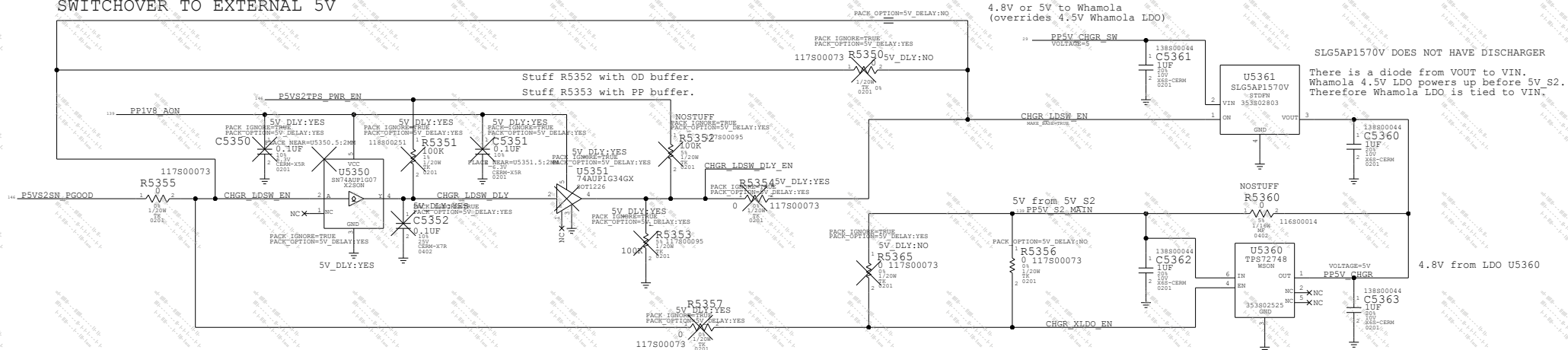


DELAY FOR 3.8V VR ENABLE- BYPASSED



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
218000505	1	RES,TK,50,6K OHM,1%,1/20W,0201	R5340	CRITICAL	JVS_DLY:YES
217800073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	R5340	CRITICAL	JVS_DLY:NO

SWITCHOVER TO EXTERNAL 5V

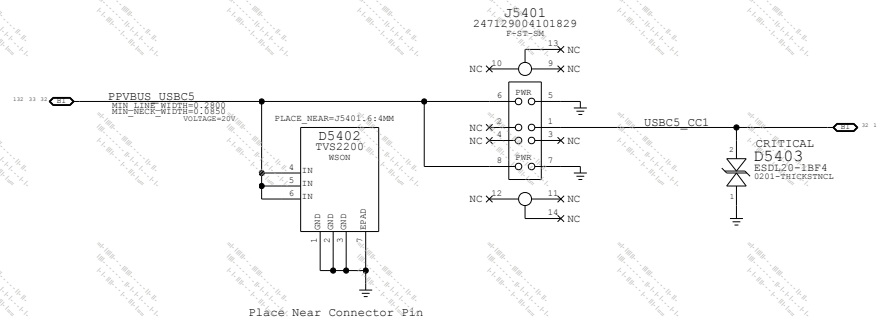


```
Load switch enable rising edge is delayed.
Load switch enable falling edge is not delayed.
LDO is enabled before the load switch is enabled.
LDO disabled to prevent 5V_S2 discharge by Q5360.
```

PAGE TITLE		DATE		PAGE	
BATTERY CHARGER SUPPORT		051-08012		D	
 Apple Inc.		REVISION		4.0.0	
NOTICE OF PROPRIETARY PROPERTY:		PART		ext-1	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY ASSET OF APPLE INC.		PAGE		53 OF 700	
IT IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.		PAGE		30 OF 159	
IT IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.		PAGE		30 OF 159	

BOM COST GROUP=BATTERY

MAGSAFE connector APN:
MLB:516S00787 / Flex:516S00788



BOM_COST_GROUP=MAGSAFE

PAGE TITLE		
MAGSAFE: CONNECTOR		
 Apple Inc.	REVISION	051-08012
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE, INC. THE REVISIONS AGREE TO THE FOLLOWING: 1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2. NOT TO REPRODUCE OR COPY IT 3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4. ALL RIGHTS RESERVED	REVISION	evt-1
	PAGE	54 OF 700
	PAGE	31 OF 159

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

D

C

B

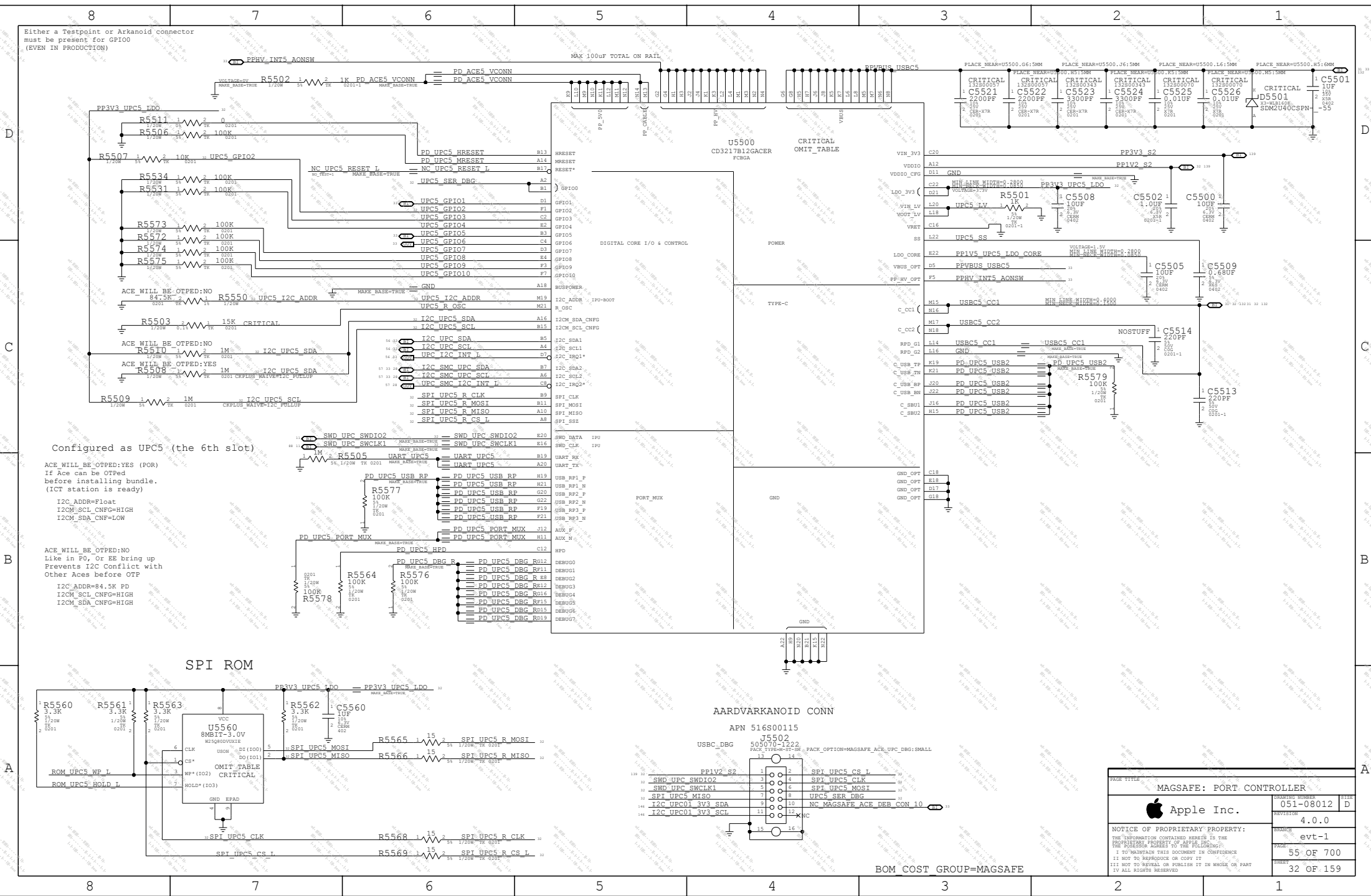
A

D

C

B

A



Configured as UPC5 (the 6th slot)

ACE_WILL_BE_OTPED:YES (POR)
If Ace can be OTped
before installing bundle.
(ICT station is ready)

I2C_ADDR=Float
I2C_SCL_CNFG=HIGH
I2C_SDA_CNFG=LOW

ACE_WILL_BE_OTPED:NO
Like in P0, Or BE bring up
Prevents I2C Conflict with
Other Aces before OTP

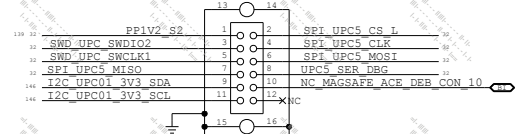
I2C_ADDR=84.5K PD
I2C_SCL_CNFG=HIGH
I2C_SDA_CNFG=HIGH

SPI ROM

AARDVARKANOID CONN

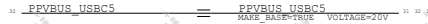
APN 516800115

USBC_DBG 505070-1222
PACK_OPTION=MAGSAFE_ACE_UPC_DBG:SMALL

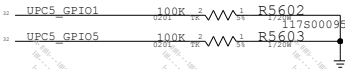


PAGE TITLE			
MAGSAFE: PORT CONTROLLER			
 Apple Inc.	REVISION	051-08012	D
	4.0.0		
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. ONE HORIZON AVENUE, CUPERTINO, CA 95014 1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2. NOT TO REPRODUCE OR COPY IT 3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4. ALL RIGHTS RESERVED	REVISION	evt-1	
	PAGE	55 OF 700	
			32 OF 159

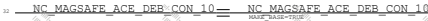
POWER ALIASES



GPIOs



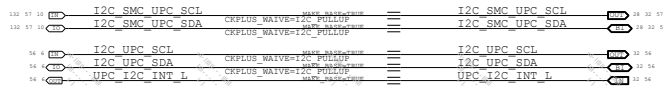
DEBUG PORT



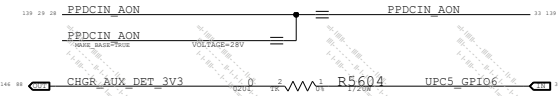
POWER / FUSE FOR UPC



I2C

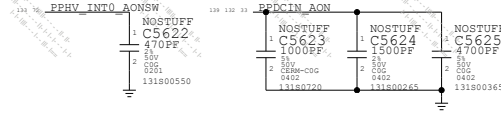


CONNECTION TO CHARGER



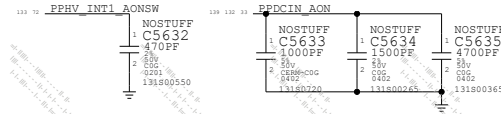
PLACE NEAR ACE0 UF400

rdar://87100189



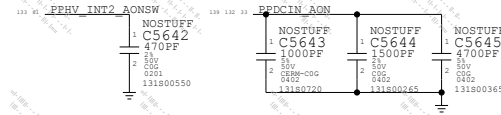
PLACE NEAR ACE1 UF500

rdar://87100189



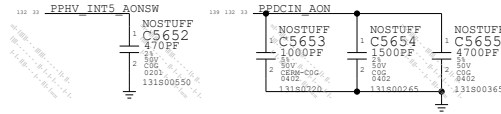
PLACE NEAR ACE2 UG400

rdar://87100189



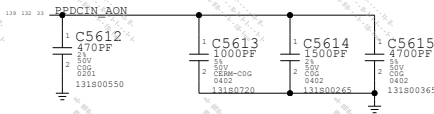
PLACE NEAR ACE5 U5500

rdar://87100189



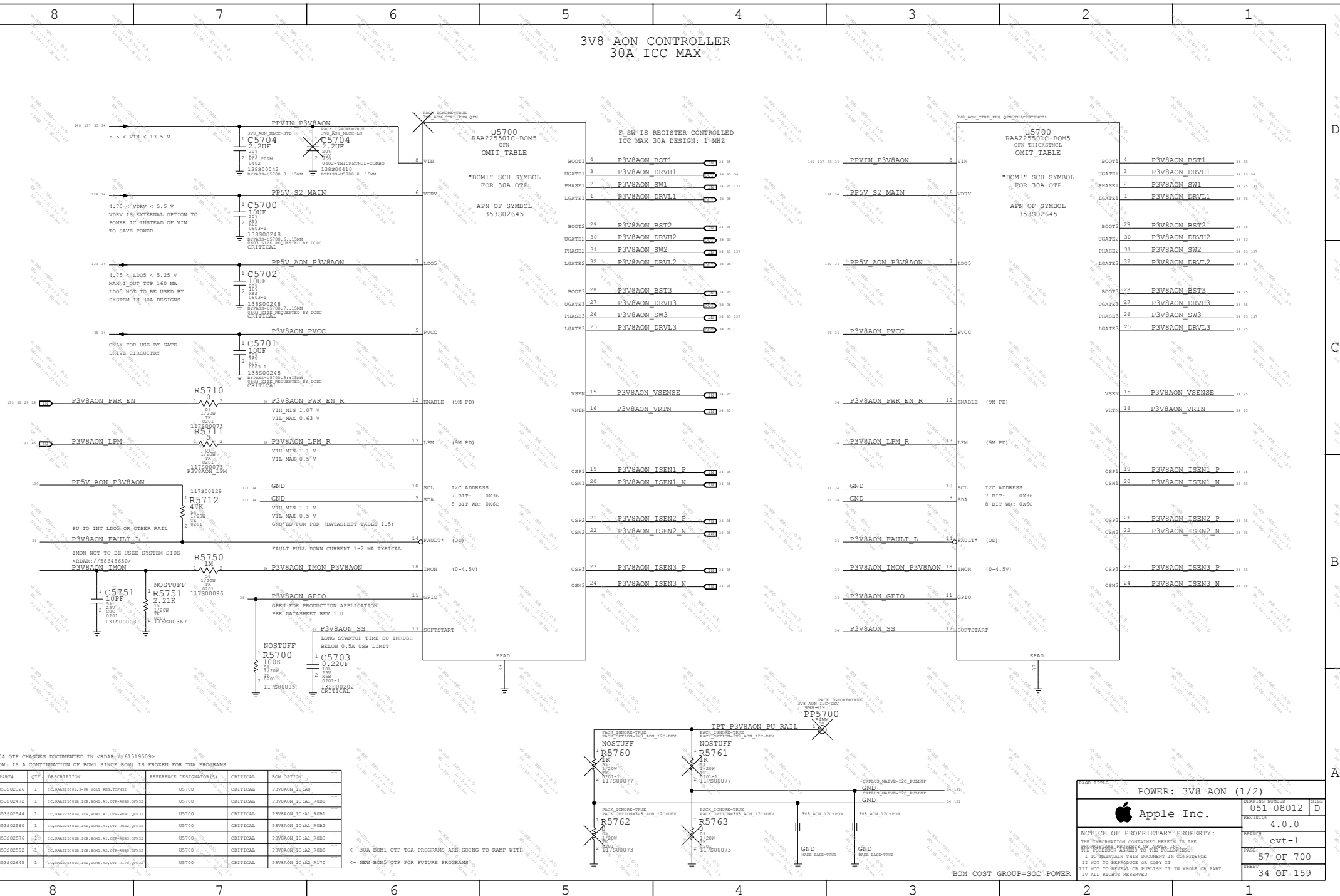
PLACE NEAR R5220

rdar://87100189



BOM_COST_GROUP=MAGSAFE

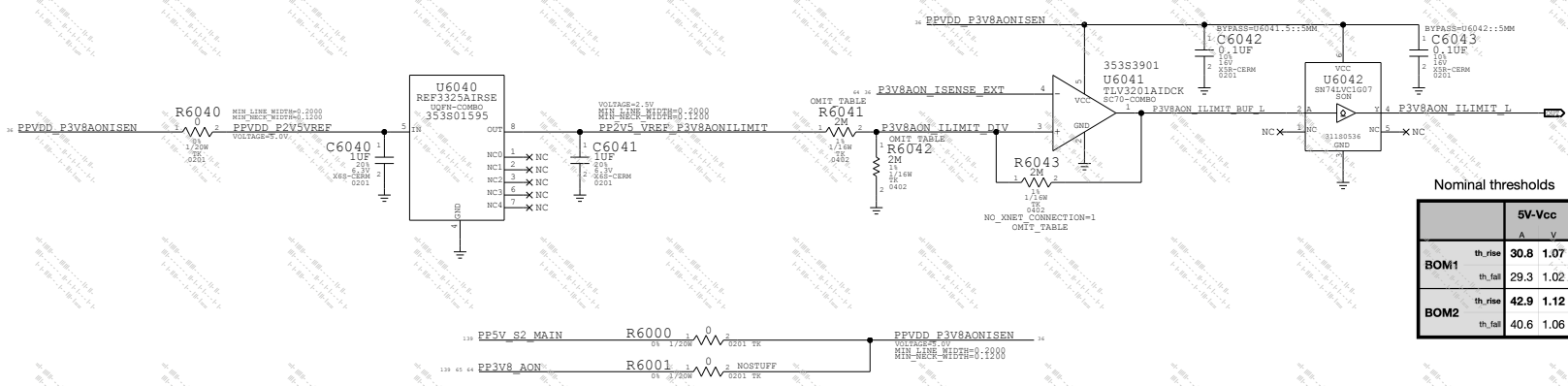
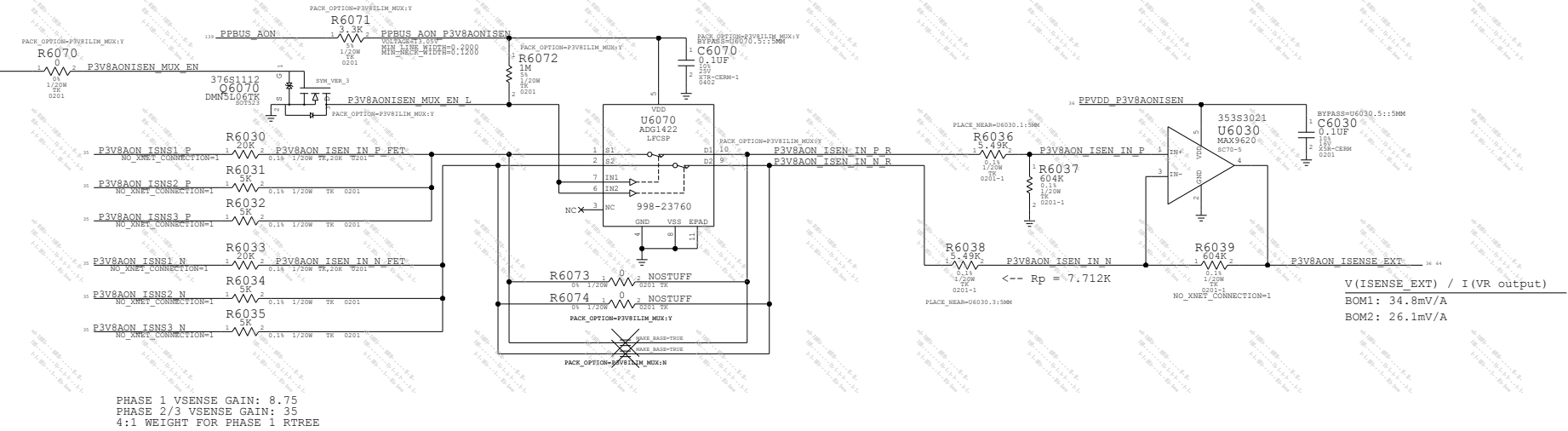
PAGE TITLE		
MAGSAFE: CONTROLLER SUPPORT		
 Apple Inc.	051-08012	D
	4.0.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE RECIPIENT AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2 NOT TO REPRODUCE OR COPY IT 3 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4 ALL RIGHTS RESERVED	evt-1	
	56 OF 700	
	33 OF 159	



P3V8 LOW SIDE ISENSE AND ILIMIT (SUMMING AMP FOR 3 PHASES)

rdar://problem/69466996 Iceman Throttle Design Data

10A MAX ON PHASE 1, MAX TOTAL CURRENT SENSE @ PMU= 43.11A



Call one of these BOM GROUPs in the main BOM:

BOM GROUP	BOM OPTIONS
P3V8ILIM:BOM1_5V	P3V8ILIM_RT:22K,P3V8ILIM_RB:15K4,P3V8ILIM_RF:866K
P3V8ILIM:BOM2_5V	P3V8ILIM_RT:20K,P3V8ILIM_RB:15K,P3V8ILIM_RF:715K

Don't Call these OPTIONS directly:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114800178	1	RES,0402,100,1/100,20K	R6041	P3V8ILIM_RT:20K
114800279	1	RES,0402,10,1/100,20K	R6041	P3V8ILIM_RT:20K
114800177	1	RES,0402,10,1/100,15K	R6042	P3V8ILIM_RB:15K
114800201	1	RES,0402,10,1/100,10.4K	R6042	P3V8ILIM_RB:10K4
114800179	1	RES,0402,10,1/100,715K	R6043	P3V8ILIM_RF:715K
114800202	1	RES,0402,10,1/100,866K	R6043	P3V8ILIM_RF:866K

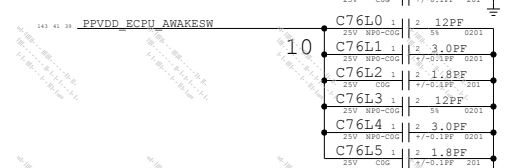
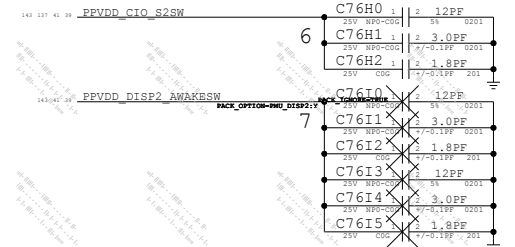
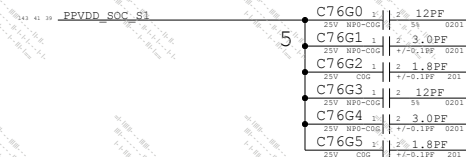
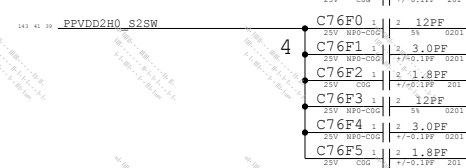
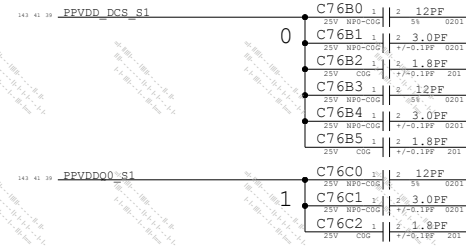
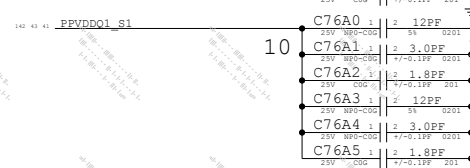
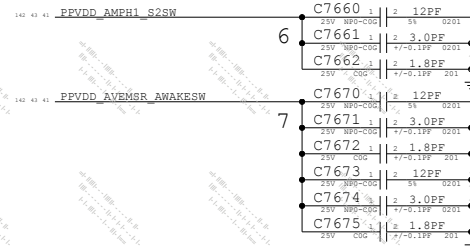
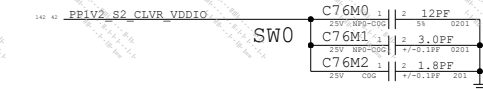
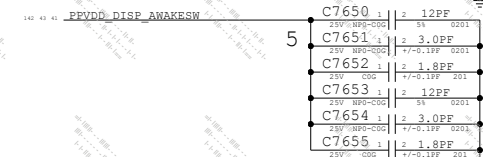
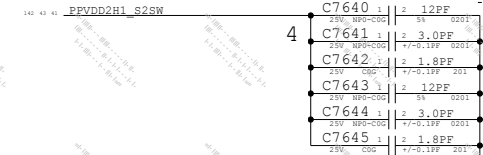
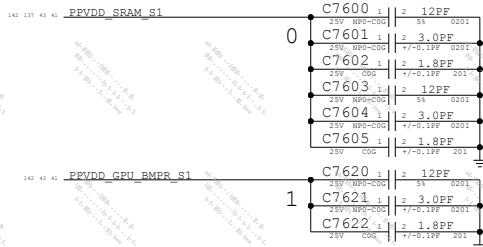
BOM_COST_GROUP=SOC_POWER

POWER: 3V8 AON OUTPUT THROTTLE		051-08012	Page D
Apple Inc.		4.0.0	
NOTICE OF PROPRIETARY PROPERTY:		evt-1	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE REVISIONS AGREE TO THE FOLLOWING:		60 OF 700	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		36 OF 159	
I NOT TO REPRODUCE OR COPY IT			
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
I TO ALL RIGHTS RESERVED			

Desense Caps for every rail
1 set for 1- and 2- phase BUCKs
2 set for 3- and 4- phase BUCKs

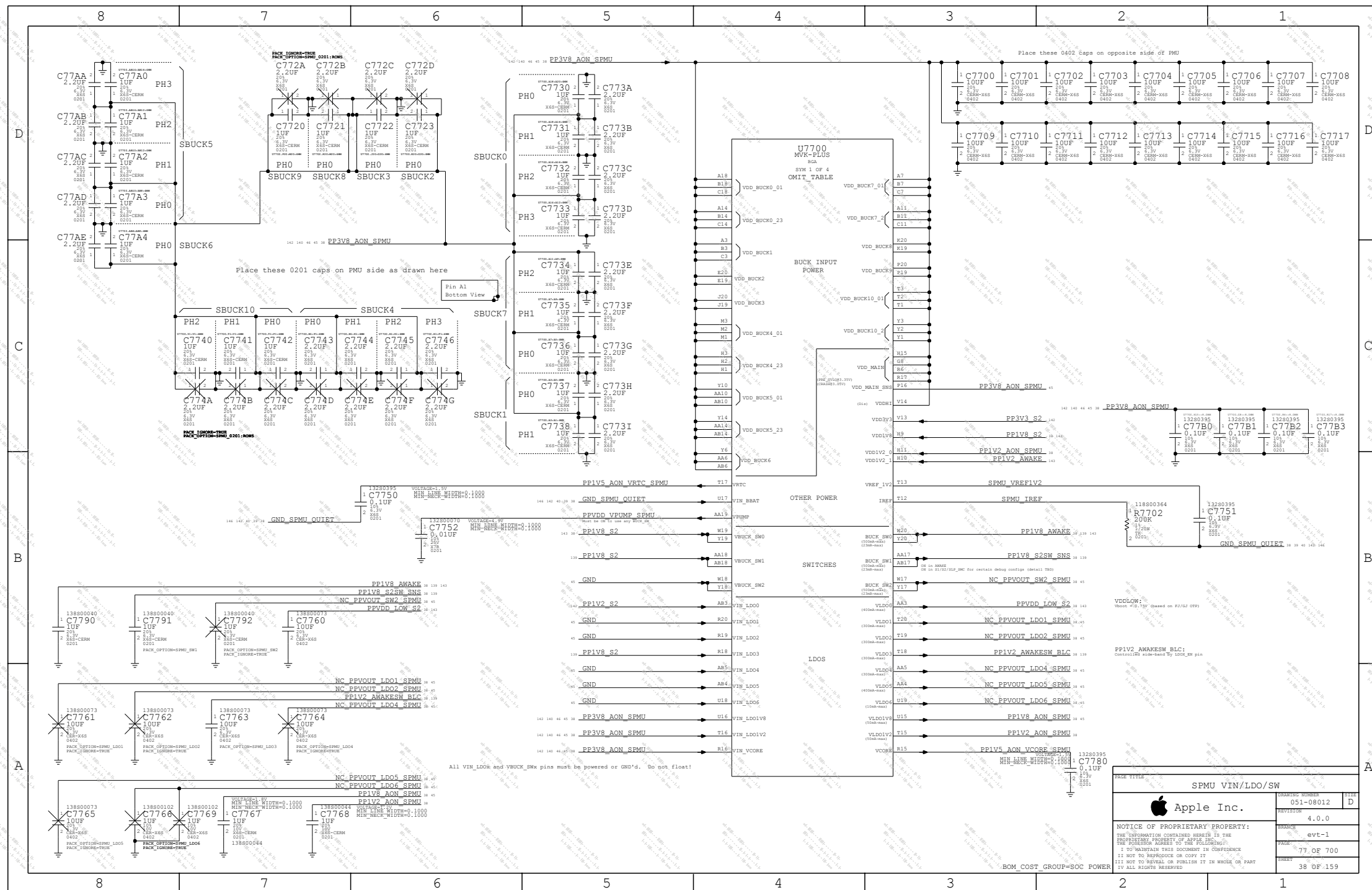
MPMU

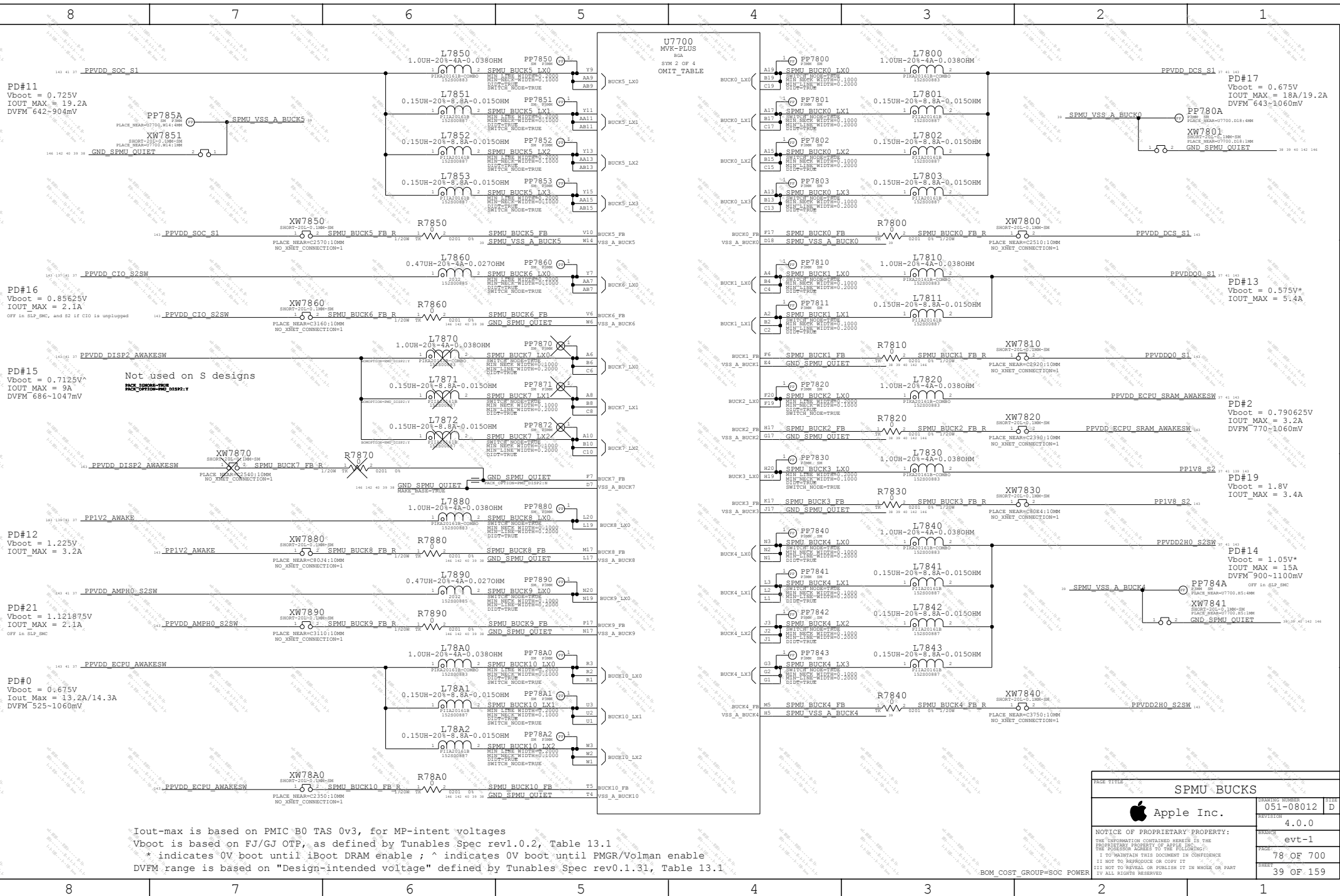
SPMU

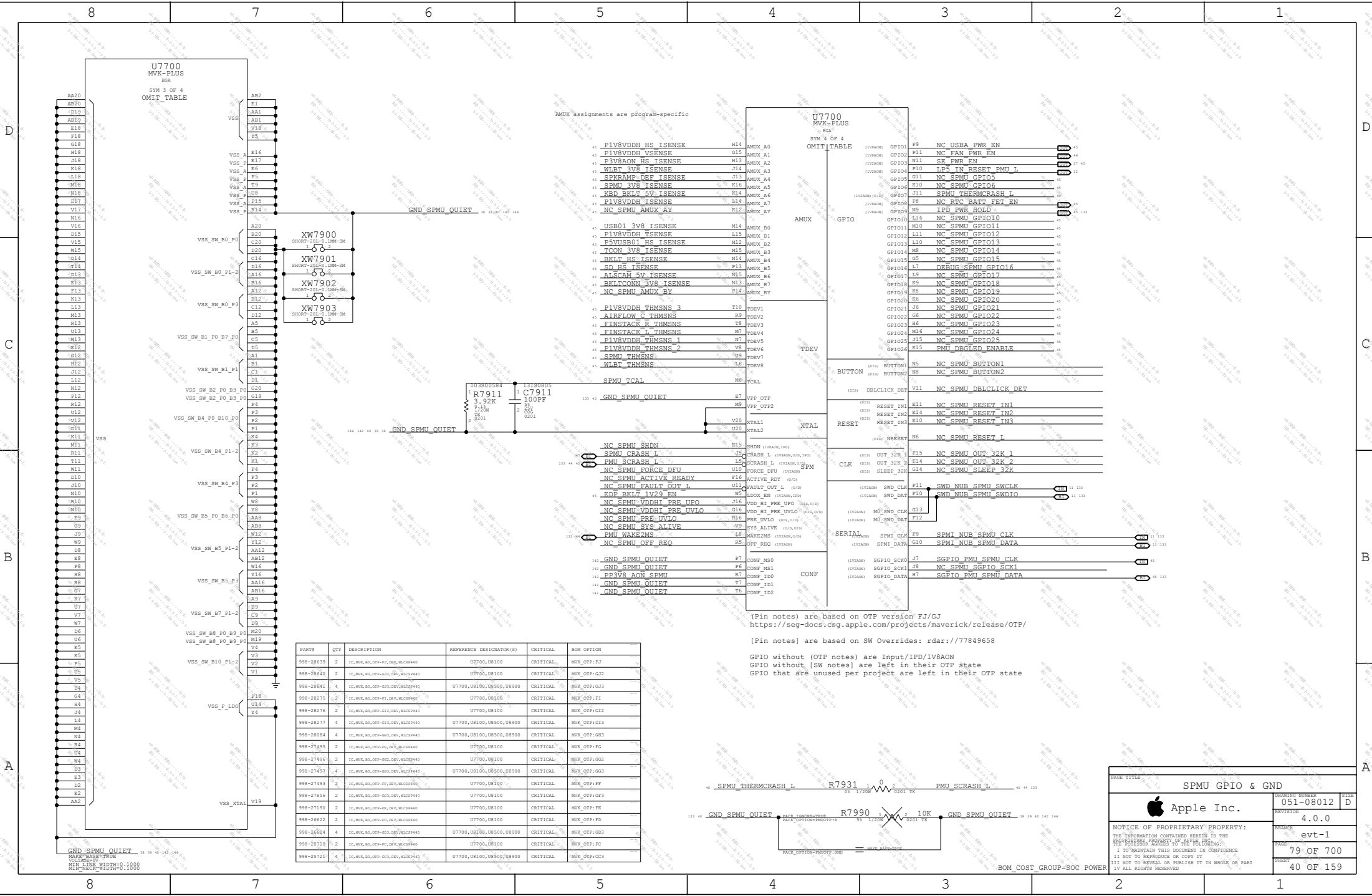


PAGE TITLE		
PMU OUTPUT DESENSE CAPS		
 Apple Inc.	REVISION	051-08012
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC. ALL RIGHTS RESERVED.	REVISION	evt-1
	PAGE	76 OF 700
	PAGE	37 OF 159

BOM_COST_GROUP=WIREFLESS

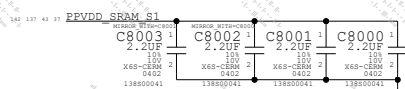




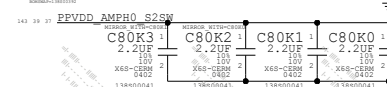
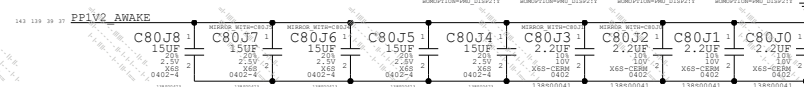
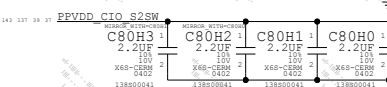
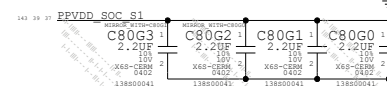
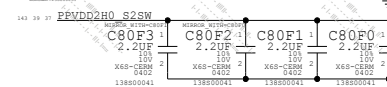
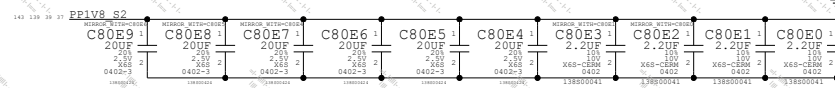
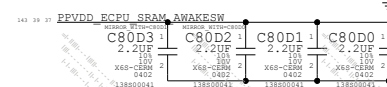
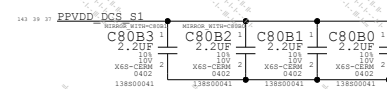
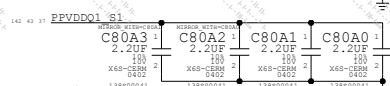
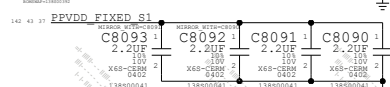
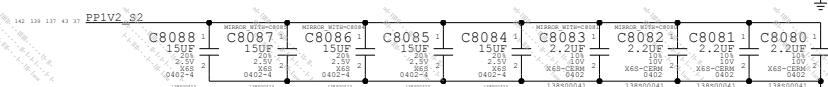
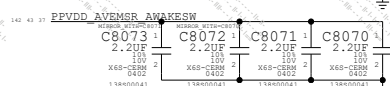
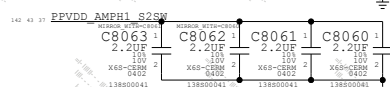
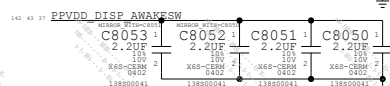
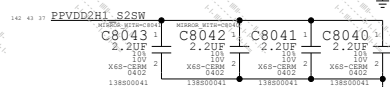
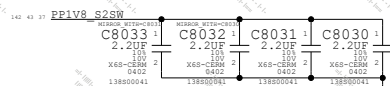


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR (S)	CRITICAL	BOM OPTION
998-28639	2	IC,MWR,M0_OTP-F2,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:F2
998-28640	2	IC,MWR,M0_OTP-G2,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:G2
998-28641	4	IC,MWR,M0_OTP-G2,DEV,M0C2P440	U7700,U8100,U8500,U8900	CRITICAL	MWR_OTP:G3
998-28275	2	IC,MWR,M0_OTP-F1,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:F1
998-28276	2	IC,MWR,M0_OTP-G2,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:G2
998-28277	4	IC,MWR,M0_OTP-G2,DEV,M0C2P440	U7700,U8100,U8500,U8900	CRITICAL	MWR_OTP:G3
998-28084	4	IC,MWR,M0_OTP-G2,DEV,M0C2P440	U7700,U8100,U8500,U8900	CRITICAL	MWR_OTP:G3
998-27495	2	IC,MWR,M0_OTP-F2,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:F2
998-27496	2	IC,MWR,M0_OTP-G2,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:G2
998-27497	4	IC,MWR,M0_OTP-G2,DEV,M0C2P440	U7700,U8100,U8500,U8900	CRITICAL	MWR_OTP:G3
998-27498	2	IC,MWR,M0_OTP-F2,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:F2
998-27856	2	IC,MWR,M0_OTP-G2,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:G2
998-27190	2	IC,MWR,M0_OTP-F2,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:F2
998-26622	2	IC,MWR,M0_OTP-F2,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:F2
998-26624	4	IC,MWR,M0_OTP-G2,DEV,M0C2P440	U7700,U8100,U8500,U8900	CRITICAL	MWR_OTP:G3
998-28718	2	IC,MWR,M0_OTP-F2,DEV,M0C2P440	U7700,U8100	CRITICAL	MWR_OTP:F2
998-23721	4	IC,MWR,M0_OTP-G2,DEV,M0C2P440	U7700,U8100,U8500,U8900	CRITICAL	MWR_OTP:G3

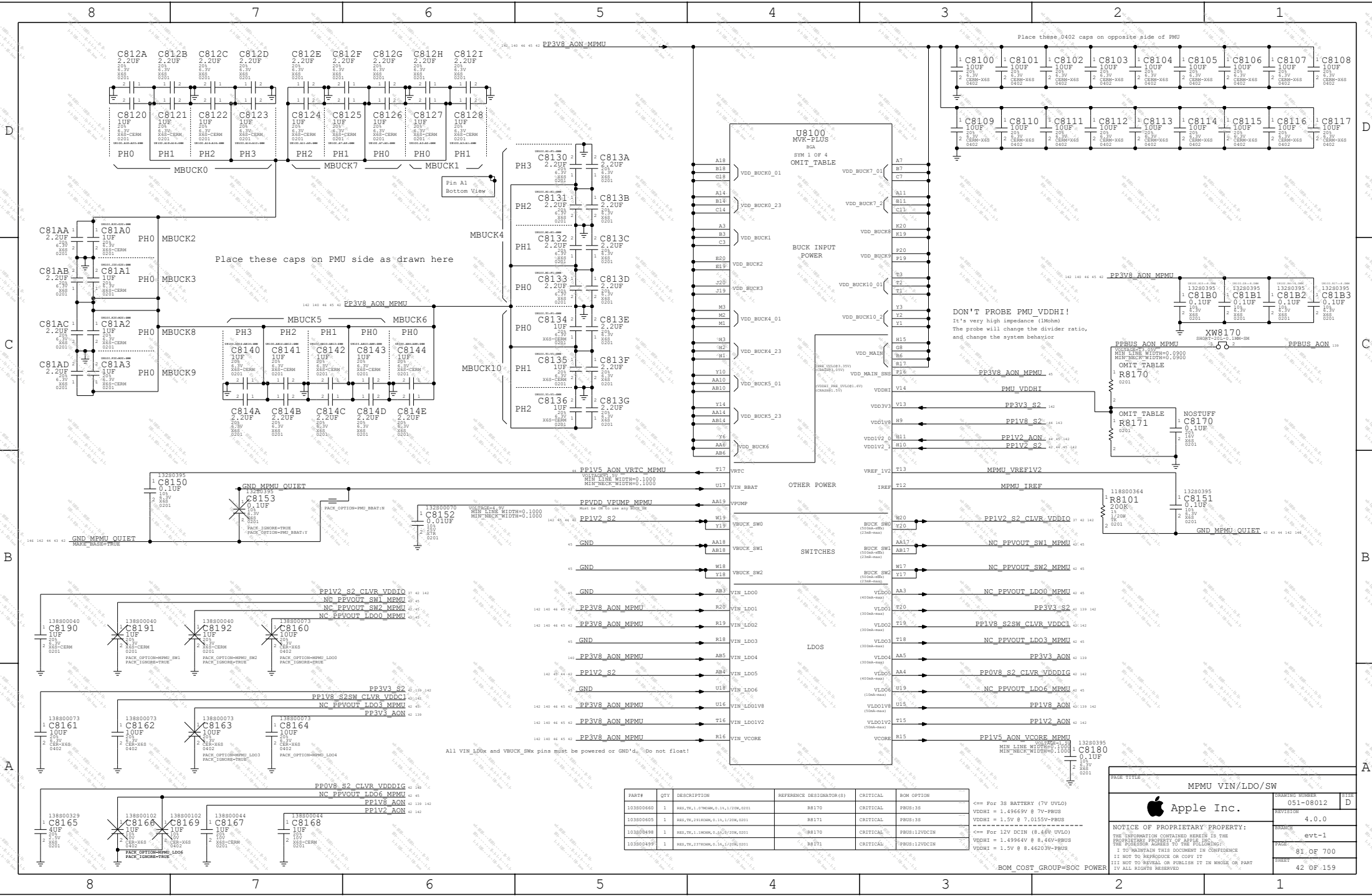
PAGE TITLE		REVISION NUMBER	DATE
SPMU GPIO & GND		051-08012	D
Apple Inc.		4.0.0	
NOTICE OF PROPRIETARY PROPERTY:		evt-1	
THIS INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE EXPRESS WRITTEN PERMISSION OF APPLE INC.		79 OF 700	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		40 OF 159	
I WILL NOT REPRODUCE OR PUBLISH IT IN WHOLE OR PART			
I WILL NOT REPRODUCE OR PUBLISH IT IN WHOLE OR PART			



<unused>



PAGE TITLE		PMU BUCK OUTPUT CAPS	
 Apple Inc.	CHANGING NUMBER	051-08012	1
	REVISION	4.0.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE EXCLUSIVE PROPERTY OF APPLE INC. AND IS NOT TO BE DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.	EXAMPLE	dev-t	
	PRICE	80.07 700	
	UNIT	41 OF 159	
	DATE		



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103800460	1	RES,7W,1.07000M,0.1%,1/20W,0201	R8170	CRITICAL	PMU:3S
103800460	1	RES,7W,2.10000M,0.1%,1/20W,0201	R8171	CRITICAL	PMU:3S
103800498	1	RES,7W,1.10000M,0.1%,1/20W,0201	R8170	CRITICAL	PMU:12VDCIN
103800499	1	RES,7W,2.10000M,0.1%,1/20W,0201	R8171	CRITICAL	PMU:12VDCIN

<= For 3S BATTERY (7V UVLO)
VDDHI = 1.49669V @ 7V-PMU
VDDHI = 1.5V @ 7.0155V-PMU

<= For 12V DCIN (8.46V UVLO)
VDDHI = 1.49664V @ 8.46V-PMU
VDDHI = 1.5V @ 8.46203V-PMU

MPMU VIN/LDO/SW

 Apple Inc.

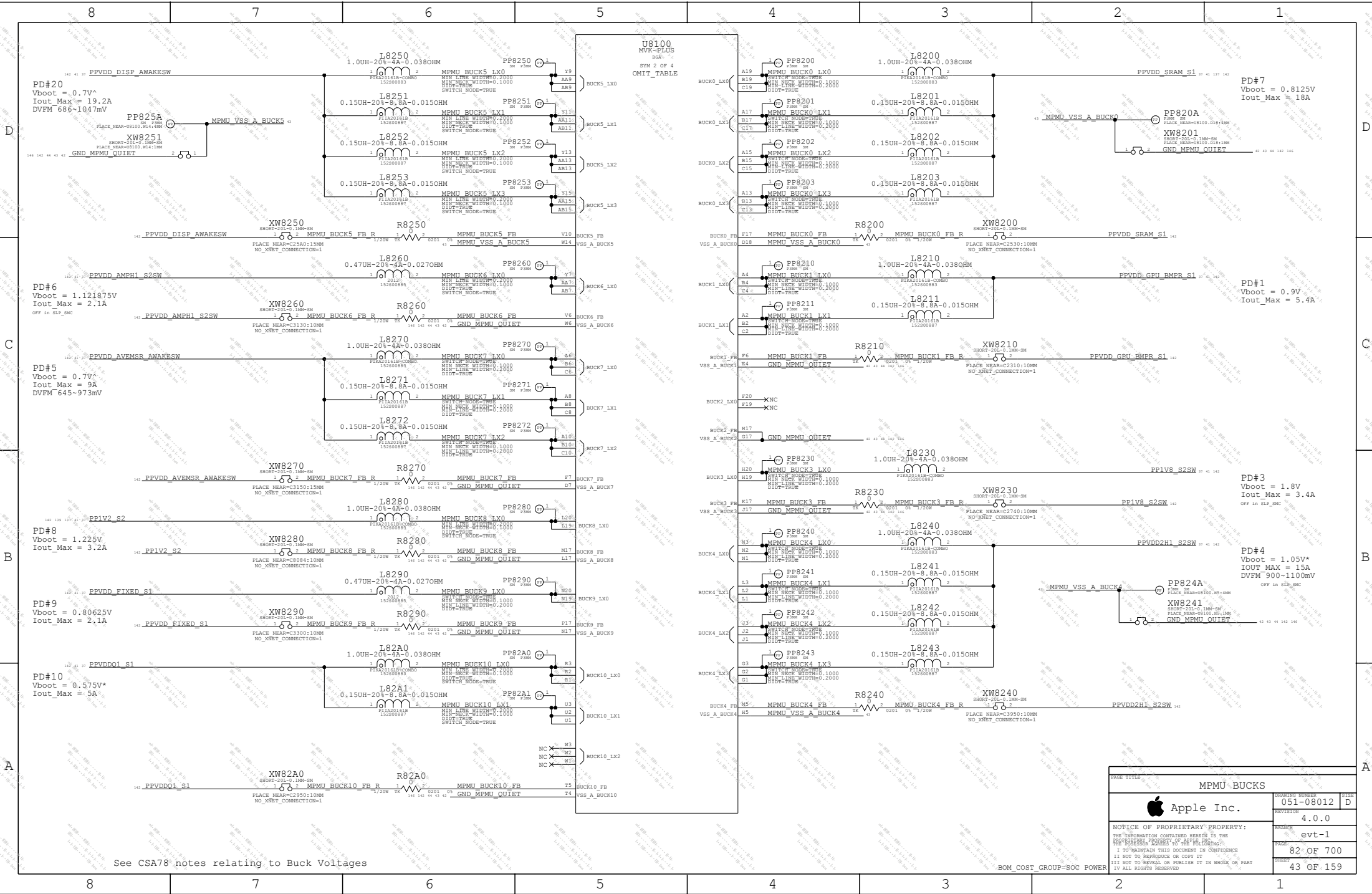
051-08012

4.0.0

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
ONE HORIZON AVENUE, CUPERTINO, CA 95014
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
1.1 NOT TO REPRODUCE OR COPY IT
1.2 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
1.3 ALL RIGHTS RESERVED

81 OF 700

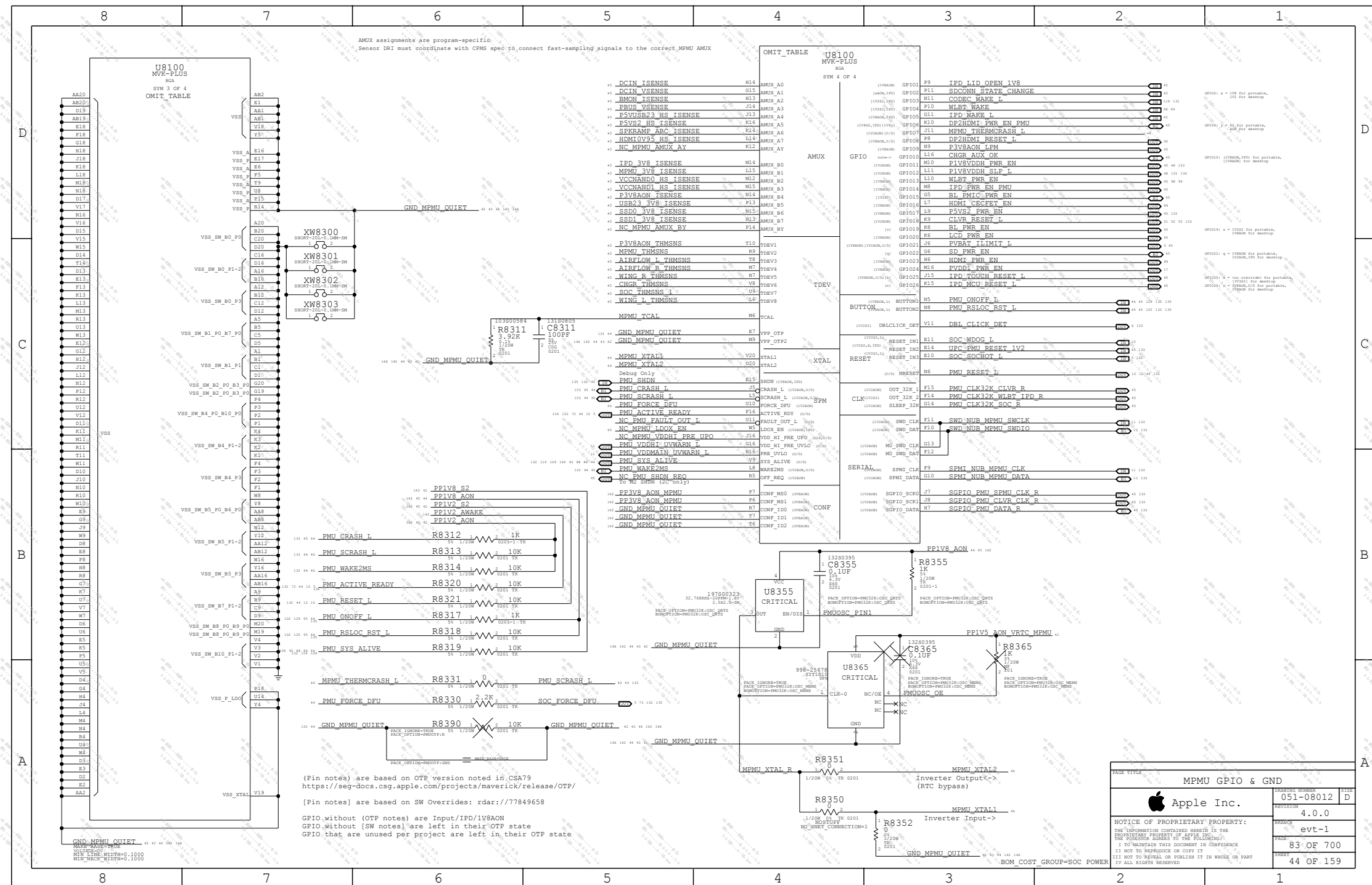
42 OF 159

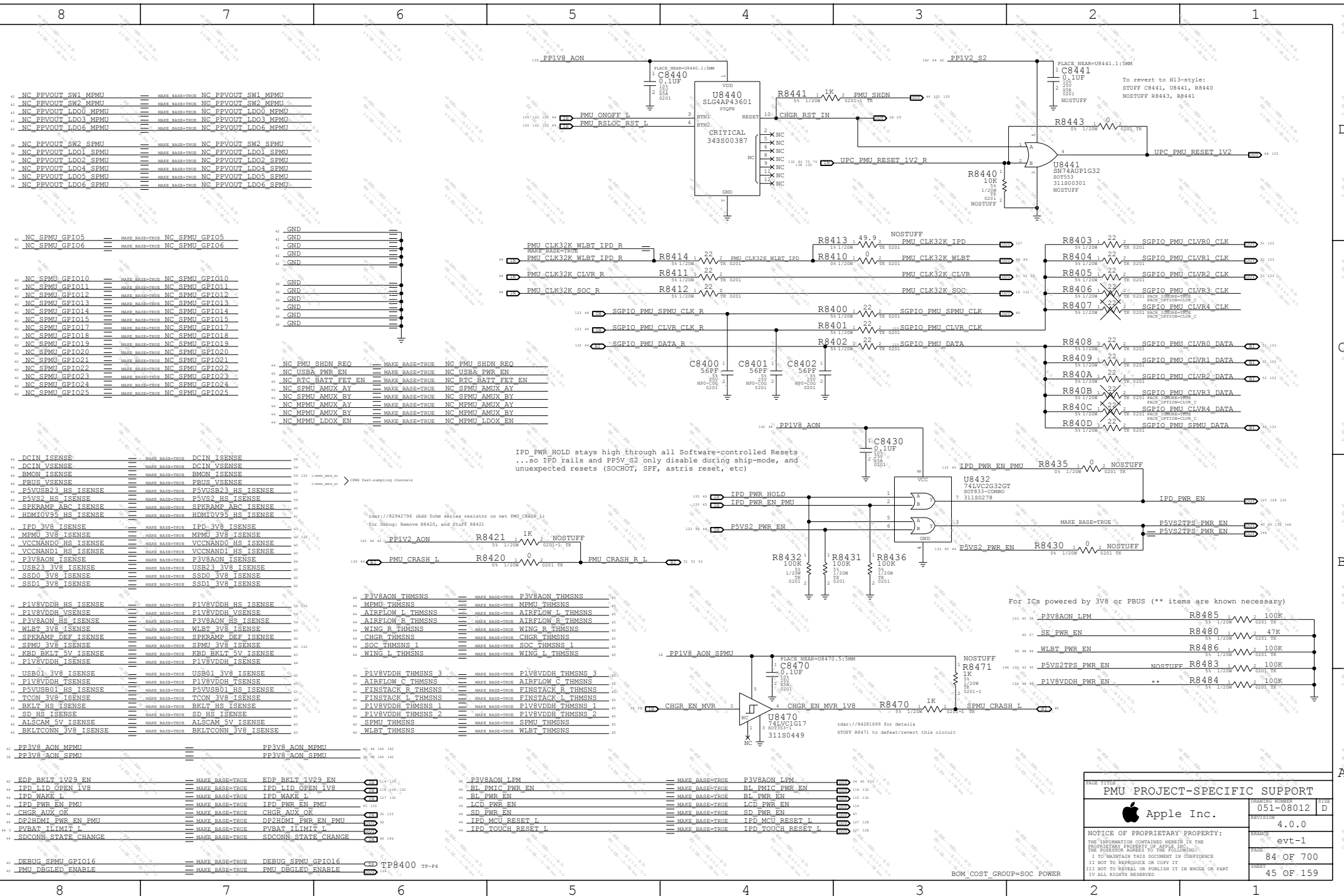


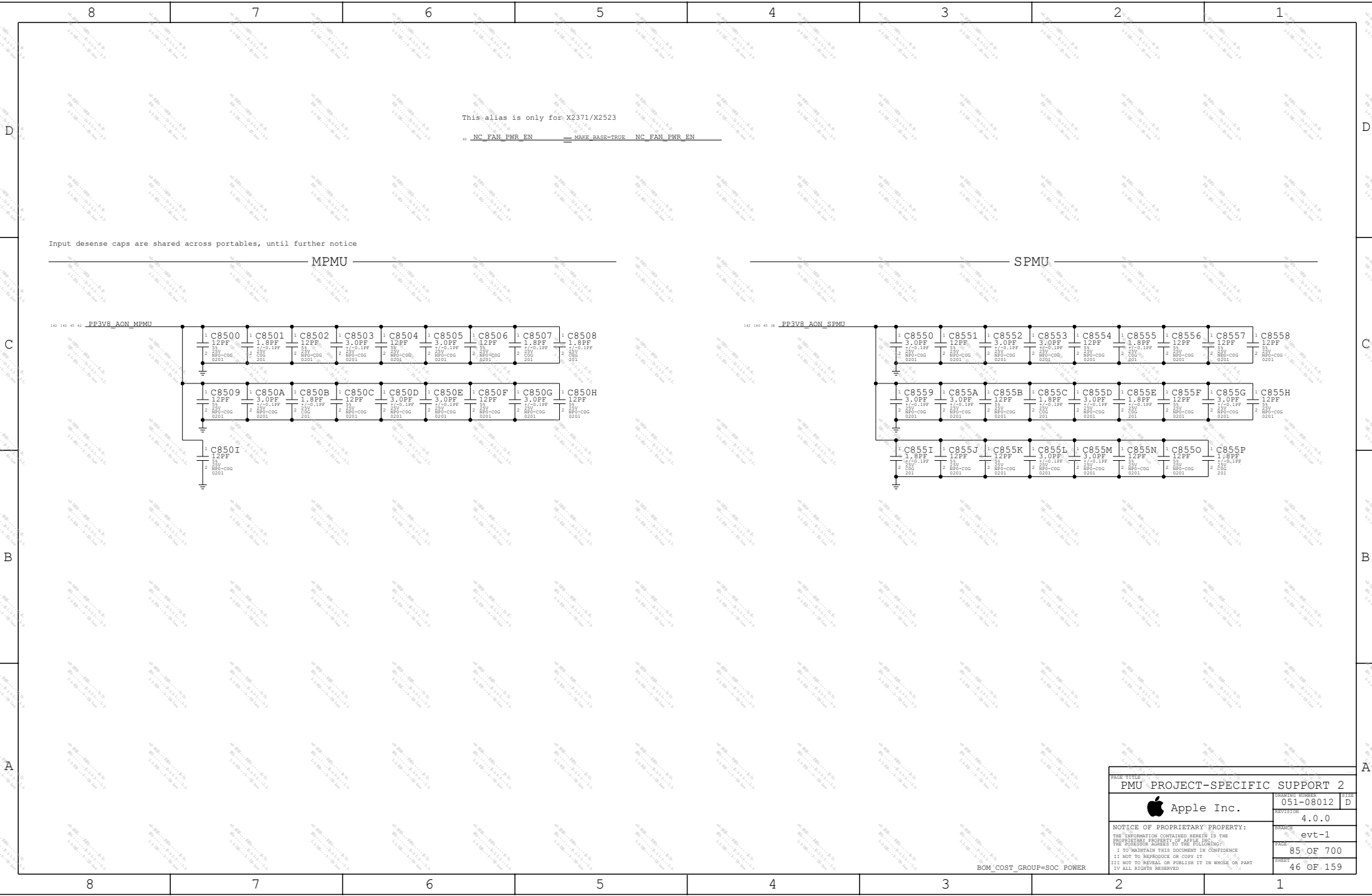
MPMU BUCKS			
 Apple Inc.	051-08012	REV	D
	4.0.0	REV	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE EXPRESS WRITTEN PERMISSION OF APPLE INC.			
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
2. NOT TO REPRODUCE OR COPIY IT			
3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
4. ALL RIGHTS RESERVED			
PAGE 82 OF 700		43 OF 159	

See CSA78 notes relating to Buck Voltages

BOM_COST_GROUP=SOC POWER







PAGE TITLE		
PMU PROJECT-SPECIFIC SUPPORT 2		
 Apple Inc.	REVISION	051-08012 D
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC. 1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2. NOT TO REPRODUCE OR COPIY IT 3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4. ALL RIGHTS RESERVED	REVISION	evt-1
	PAGE	85 OF 700
BOM_COST_GROUP=SOC POWER		46 OF 159

DUE TO PHASES NOT PLACED TOGETHER, START WITH 9X 33UF INPUT PER PHASE
ADD CAPS HERE TO AUGMENT REFERENCE DESIGN CAPS
POTENTIALLY NOSTUFF/REMOVE CAPS AFTER PLACEMENT/SIMS



moved to CSA95

ADD 2.5X 180UF OUTPUT CAPS PER 1X 470UF REMOVED FROM REFERENCE DESIGN
PLUS 1X NOSTUFF 180UF (AND 1X NOSTUFF 470UF ON CSA95)

ADDITIONAL INPUT DESENSE CAPS
PPVIN_P1V8VDDH 59 14

ADDITIONAL OUTPUT DESENSE CAPS



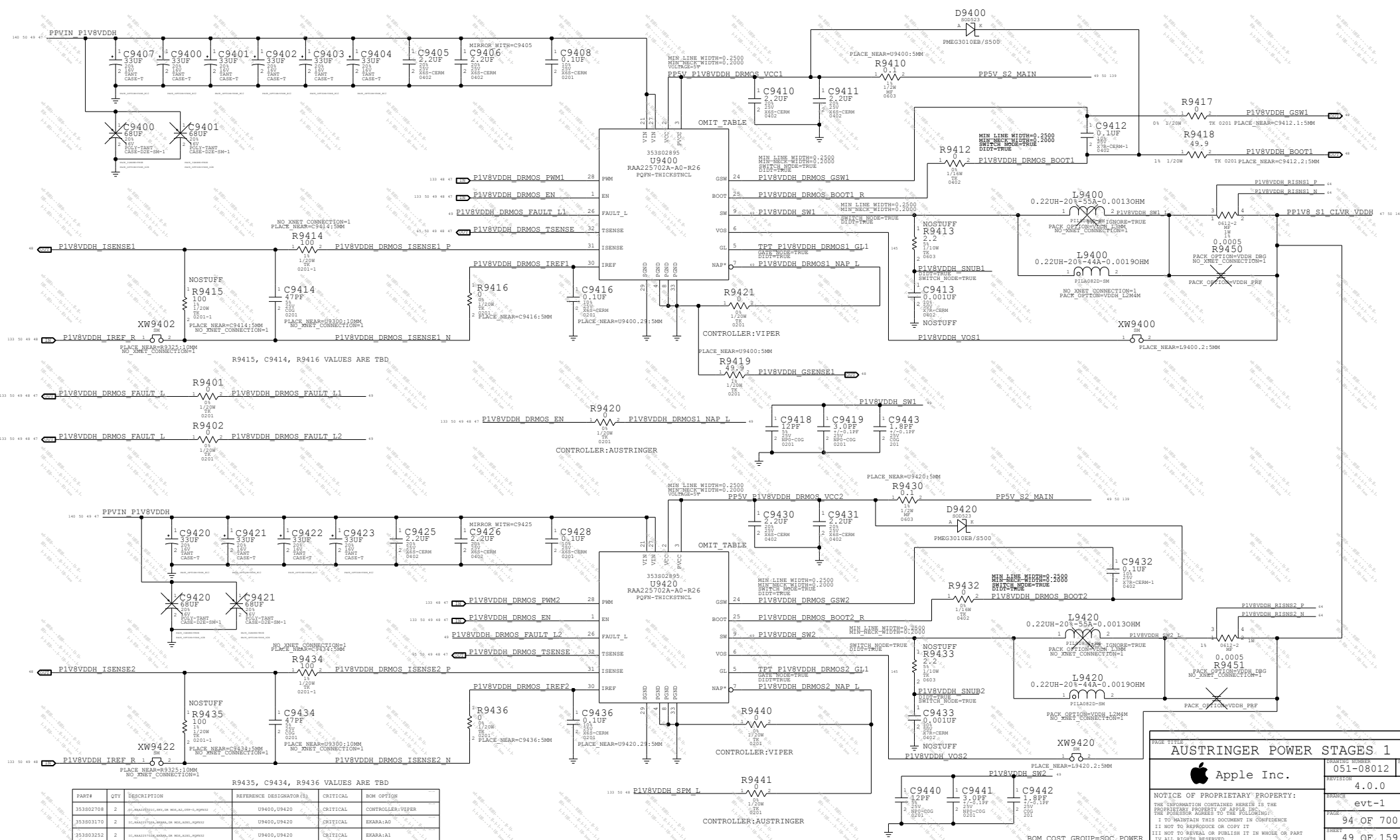
PAGE TITLE		AUSTRINGER SUPPORT	
 Apple Inc.	051-08012	D	
	4.0.0		
	evt-1		
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT THE WRITTEN CONSENT OF APPLE INC.			
TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 1) NOT TO REPRODUCE OR COPY IT 2) NOT TO DISCLOSE OR REVEAL IT 3) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART TO ANY THIRD PARTY			
PAGE		92 OF 700	
FREE		47 OF 159	

AUSTRINGER CONTROLLER



PAGE TITLE		AUSTRINGER CONTROLLER	
	Apple Inc.		
	NOTICE OF PROPRIETARY PROPERTY:		
	THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.		
	THIS DOCUMENT IS UNCLASSIFIED		
	DATE 08-09-2011 BY 60322 UCBAW		
CLASSIFICATION		01-08012	FORM D
REVISION		4.0.0	
SOURCE		evt-1	
PAGE		93 OF 700	
PAGE		48 OF 159	

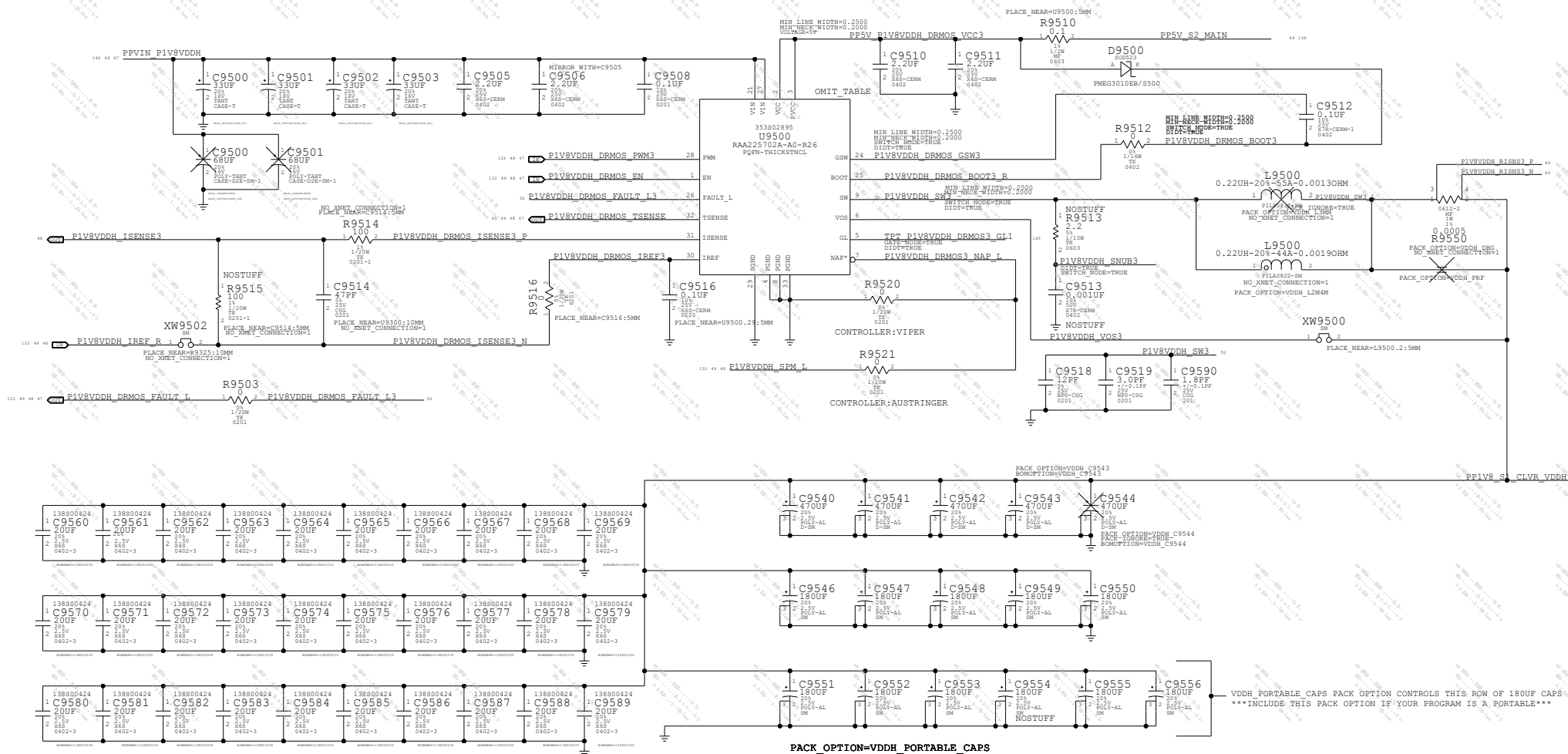
AUSTRINGER POWER STAGES 1



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353902708	2	IC,AA121111C,8V,18, 805,4A,CTP-1,PQFN32	U9400,U9420	CRITICAL	CONTROLLER:VLEP
353903170	2	IC,AA121111A,8V,805,4A,1A1,1,PQFN32	U9400,U9420	CRITICAL	EKARA:A0
353903252	2	IC,AA121111B,8V,805,4A,1A1,1,PQFN32	U9400,U9420	CRITICAL	EKARA:A1

PAGE TITLE		AUSTERLINGER POWER STAGES 1	
 Apple Inc.	DATE OF REVISION	051-08012	D
	REVISION	4.0.0	
	NOTICE OF PROPRIETARY PROPERTY:		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. ANY DISCLOSURE AGAINST THE FOLLOWING:			
1. TO MAINTAIN THIS DOCUMENT IN CONFERENCE		BRANCH	evt-1
1. IT NOT TO REPRODUCE OR COPY IT		PAGE	94 OF 700
1. IT NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		SHEET	49 OF 159

AUSTRINGER POWER STAGES 2



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353803170	1	IC,ANALOG7CH,ADCON,AD,16,PQFN32	U9500	CRITICAL	EXARA:A0
353802708	1	IC,ANALOG7CH,ADCON,AD,16,PQFN32	U9500	CRITICAL	CONTROLLER:VIPER
353803252	1	IC,ANALOG7CH,ADCON,AD,16,PQFN32	U9500	CRITICAL	EXARA:A1

PAGE TITLE		DRAWING NUMBER	
AUSTRINGER POWER STAGES 2		051-08012	
 Apple Inc.		REVISION	
		4.0.0	
NOTICE OF PROPRIETARY PROPERTY:		DRAWING	
THE INFORMATION CONTAINED HEREIN IS THE		evt-1	
PROPRIETARY PROPERTY OF APPLE INC.		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		95 OF 700	
IT NOT TO REPRODUCE OR COPY IT		SHEET	
IT NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		50 OF 159	

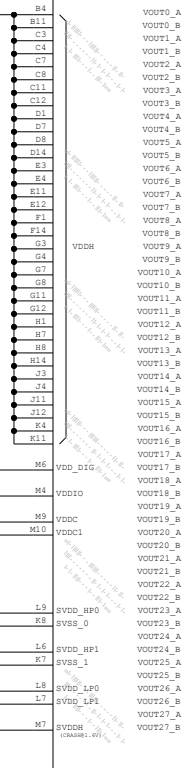
BOM COST GROUP=SOC POWER

OK2INTEGRATE

INSTANCE = C0
CFG = D (12+2+12+2)
OTP = MP_

OMIT_TABLE

UA100
MIRABEAU
FCCSR
SYM 1 OF 2



BUCK0/HP0
Vboot=0V

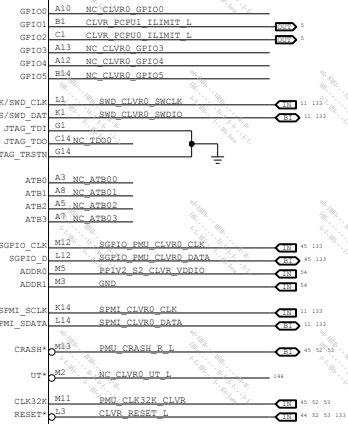
BUCK1/LP0
Vboot=0V

BUCK2/HP1
Vboot=0V

BUCK3/LP1
Vboot=0V

OMIT_TABLE

UA100
MIRABEAU
FCCSR
SYM 2 OF 2



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-28851	2	IC: MIRRABEAU, AS, OTP-HQS	UA100	CRITICAL	
998-28851	1	IC: MIRRABEAU, AS, OTP-HQS	UA700	CRITICAL	MIRABEAU_0

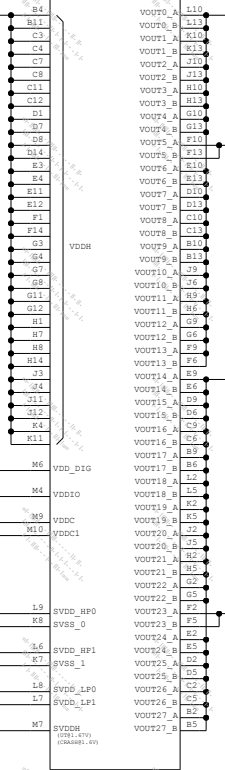
CLVR0		
 Apple Inc.	051-08012	DATE D
	4.0.0	REVISION
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. IT IS TO BE KEPT CONFIDENTIAL AND NOT TO BE REPRODUCED OR DISCLOSED TO ANY OTHER PARTY WITHOUT THE WRITTEN PERMISSION OF APPLE INC.		101 OF 700
BOM_COST_GROUP=SOC POWER		51 OF 159

OK2INTEGRATE

INSTANCE = C1
CFG = A (13+1+13+1)
OTP = AP_

OMIT TABLE

UA200
MIRABEAU
VCCSF
SYM 1 OF 2



BUCK0/HP0
Vboot=0V

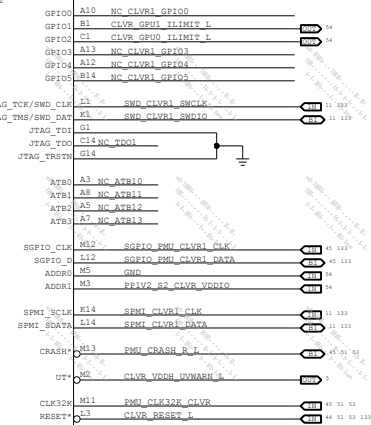
BUCK1/LP0
Vboot=0V

BUCK2/HP1
Vboot=0V

BUCK3/LP1
Vboot=0V

OMIT TABLE

UA200
MIRABEAU
VCCSF
SYM 2 OF 2



VSS

VSSC

KEEP BELOW 25 OHM FOR ONE SVDDH

FILTER CUTOFF: 15MHZ

TODO_DT: Update with APN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-28849	1	TC;Mirabeau_M0_OTP-APG	UA200	CRITICAL	
998-28849	1	TC;Mirabeau_M0_OTP-APG	UA300	CRITICAL	MIRABEAU_C
998-28849	3	TC;Mirabeau_M0_OTP-APG	UA300,UA800,UA900	CRITICAL	MIRABEAU_S

BOM_COST_GROUP=SOC POWER

CLVR1		
 Apple Inc.	DESIGN NUMBER	051-08012
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY:		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE REVISIONS AGREE TO THE FOLLOWING:		
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		
2. NOT TO REPRODUCE OR COPY IT		
3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		
4. ALL RIGHTS RESERVED		
REVISION	evt-1	
PAGE	102 OF 700	
SHEET	52 OF 159	

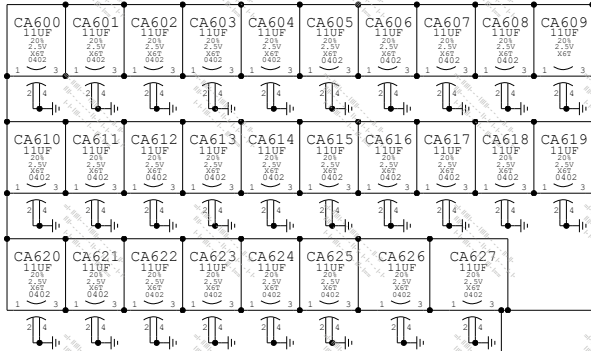
OK2 INTEGRATE

TODO DT: Quantity of desense and 11uF VDDH caps is still TBD based on layout study. Baseline is from X2724/X2728 quantity
TODO DT: Potentially add or remove, or PACK OPTION some desense input caps based on layout

FP1V8_S1_CLVR_VDDH 11uF 50 140

11uF APN: 138S00328

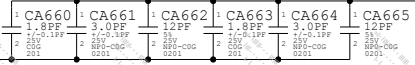
INSTANCE = C2
CFG = C (8+1+13+6)
OTP = IP_



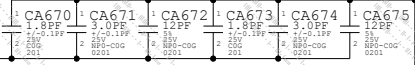
CLVR0



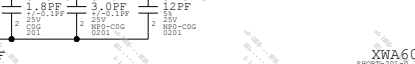
CLVR1



CLVR2



CA676 CA677 CA678



XWA600

SHORT=20L-0.18M-SM

1 2

XWA601

SHORT=20L-0.18M-SM

1 2

140 51 51

FP1V8_S2_CLVR_VDD1G

140 14 30 51

FP1V2_S2_CLVR_VDDIO

140 52 51

FP1V8_S2R8

140 52 51

FP1V8_S2R8_CLVR_VDDC1

140 52 51

FPVDDANR_FR

140 52 51

FPVDDFABRIC_FR

140 52 51

FPVDDANESRAM_FR

140 52 51

FPVDDAFRCS_FR

140 52 51

FP1V8_S1_CLVR_VDDH

140 52 51

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

FPVDDANESRAM_FR

140 51 51

FPVDDAFRCS_FR

140 51 51

FP1V8_S1_CLVR_VDDH

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

140 51 51

140 51 51

FPVDDANR_FR

140 51 51

FPVDDFABRIC_FR

D

C

B

A

CLVR Throttle Probe Access (Different between S,C,D)



CLVR Address Straps (Different between S vs C/D)

SWD TINSTANCE and SGPIO SID are the same value within a given CLVR
ADDR[1:0] define LSB
OTP defines MSB

CLVR	Hex	MSB OTP	LSB ADDR straps		
0	0x1	b00	b01 :	51 52 53 54 140	51 52 53 54 140
1	0x2	b00	b10 :	51 52 53 54 142	51 52 53 54 142
2	0x9	b10	b01 :	51 52 53 54 142	51 52 53 54 142

BOM_COST_GROUP=SQC POWER

PAGE TITLE		
CLVR PROJECT SUPPORT (S)		
 Apple Inc.	051-08012	PAGE D
	4.0.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE, INC. THE RECIPIENT AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED		
	118 OF 700	
	54 OF 159	

* OK2INTEGRATE *

5V_S2 VR

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=5V_S2_PBUS-18V
PACK_OPTION=5V_S2_PBUS-B12
PACK_OPTION=5V_S2_PBUS-D2
PACK_OPTION=5V_S2_PBUS-D12
PACK_OPTION=5V_S2_PBUS-25V_D2

Start up time
min=4.3ms
typ=6.4ms
max=8.81ms

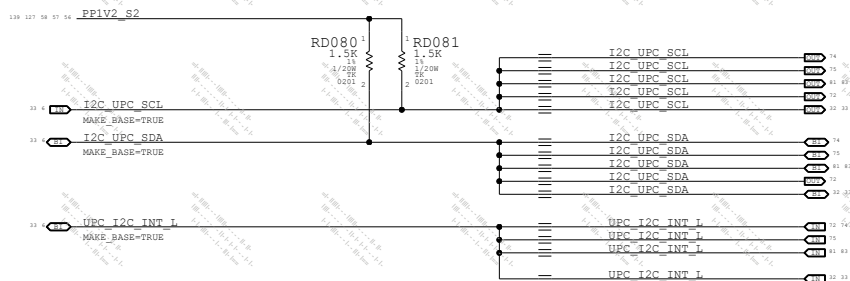
VOUT=5.15V
EDC=3.0A
F=1.5MHz

Decay time to 0.1V
min=100ms
typ=132ms
max=166ms

PAGE TITLE		
POWER: 5V S2		
 Apple Inc.	REVISION	051-08012
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.	REVISION	evt-1
	REVISION	122 OF 700
BOM_COST_GROUP=PLATFORM POWER		55 OF 159

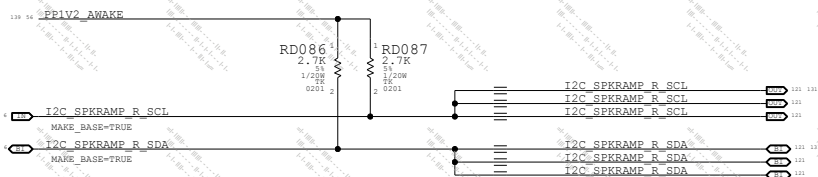
AP_I2C0

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	0	380kHz	0x38	0x70	ACE2 - 0 (DEMOG)
AP	0	380kHz	0x3F	0x7E	ACE2 - 1 (DEMOG)
AP	0	380kHz	0x3B	0x76	ACE2 - 2 (DEMOG)
AP	0	380kHz	0x3A	0x74	ACE2 - 5 (DEMOG)
AP	0	380kHz	0x6B	0xD6	BANK ALL CALL



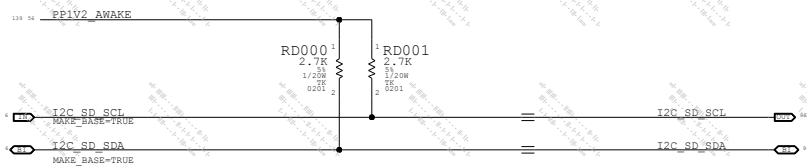
AP_I2C3

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	3	400kHz	0x3B	0x76	SPKRAMP_TANANG_D
AP	3	400kHz	0x3C	0x78	SPKRAMP_TANANG_E
AP	3	400kHz	0x3D	0x7A	SPKRAMP_TANANG_F



AP_I2C4

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	4	400kHz	0x6A	0xD4	SDCARD

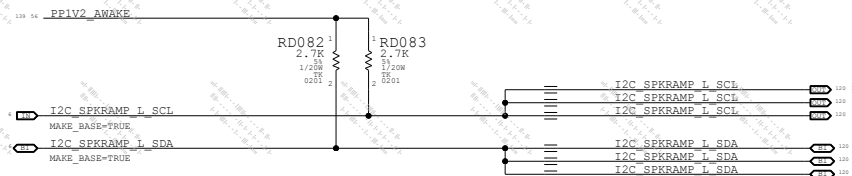


UNUSED:

AP_I2C0
ISP_I2C0
ISP_I2C1
ISP_I2C3

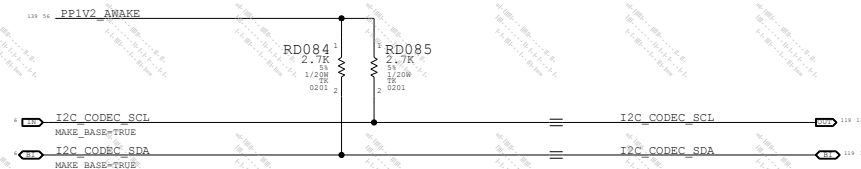
AP_I2C1

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	1	400kHz	0x38	0x70	SPKRAMP_TANANG_A
AP	1	400kHz	0x39	0x72	SPKRAMP_TANANG_B
AP	1	400kHz	0x3A	0x74	SPKRAMP_TANANG_C



AP_I2C2

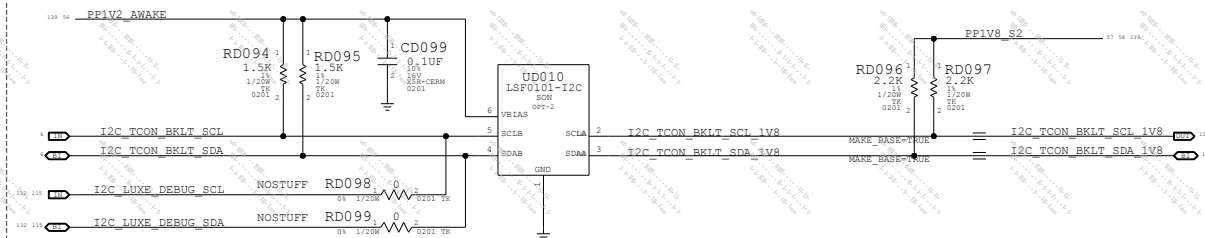
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	2	400kHz	0x4B	0x90	CODEC - CLIFDEN
AP	2	400kHz	0x4B	0x95	CODEC - CARLOW (FOR



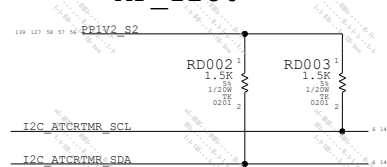
AP_I2C7

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	7	1MHz	0xXX	0xX	Avellino PMIC

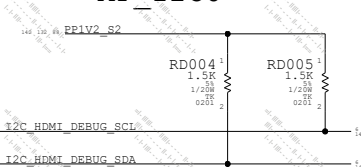
I2C is hooked up to testpoints on BCON brd



AP_I2C6



AP_I2C8



I2C Connections - AP

Apple Inc.	051-08012	D
4.0.0		
evt-1		
130 OF 700		
56 OF 159		

8

7

6

5

4

3

2

1

PPIV2_S2

CD102 1
0.1uF
100
X5R-CERM
0201

RD174 1
10K
1/20W
0201

RD175 1
10K
1/20W
0201

UD102
LSF0101-I2C
SON
OFF-2

RD177 1
3.3K
1/20W
0201

RD178 1
3.3K
1/20W
0201

PPIV8_S2

RD153 1
0
1/20W
0201

RD154 1
0
1/20W
0201

SMC_I2C0

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	0	400kHz	0X09	0X12	CHARGER - S00NA
SMC	0	400kHz	0X09	0X12	CHARGER - W00MOLA
SMC	0	400kHz	0X0B	0X16	BMU

SMC_I2C1

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	1	100kHz/400kHz	0X38	0X70	ACK2 - 0 (DEBGG)
SMC	1	100kHz/400kHz	0X3F	0X7E	ACK2 - 1 (DEBGG)
SMC	1	100kHz/400kHz	0X3B	0X76	ACK2 - 2 (DEBGG)
SMC	1	100kHz/400kHz	0X3A	0X74	ACK2 - 5 (DEBGG)
SMC	1	100kHz/400kHz	0X6B	0XD6	BANK1 ALL CALL

SMC_I2C2

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	2	100kHz	0X79	0XF2	NAND PMIC_0
SMC	2	100kHz	0X78	0XF0	NAND PMIC_1

PPIV2_S2

RD190 1
1.5K
1/20W
0201

RD191 1
1.5K
1/20W
0201

I2C_SMC_UPC_SCL
MAKE_BASE=TRUE

I2C_SMC_UPC_SDA
MAKE_BASE=TRUE

UPC_SMC_I2C_INT_L
MAKE_BASE=TRUE

I2C_SMC_UPC_SCL
I2C_SMC_UPC_SCL
I2C_SMC_UPC_SCL
I2C_SMC_UPC_SCL
I2C_SMC_UPC_SDA
I2C_SMC_UPC_SDA
I2C_SMC_UPC_SDA
I2C_SMC_UPC_SDA
I2C_SMC_UPC_SDA

UPC_SMC_I2C_INT_L
UPC_SMC_I2C_INT_L
UPC_SMC_I2C_INT_L
UPC_SMC_I2C_INT_L

PPIV2_S2

RD130 1
1.5K
1/20W
0201

RD131 1
1.5K
1/20W
0201

CD103 1
0.1uF
100
X5R-CERM
0201

UD104
LSF0101-I2C
SON
OFF-2

PPIV8_S2

RD133 1
2.2K
1/20W
0201

RD132 1
2.2K
1/20W
0201

I2C_SMC_NAND_SCL
I2C_SMC_NAND_SDA

I2C_NAND_PMIC_SCL_1V8
I2C_NAND_PMIC_SDA_1V8
MAKE_BASE=TRUE
MAKE_BASE=TRUE

I2C_NAND_PMIC_SCL_1V8
I2C_NAND_PMIC_SDA_1V8

BOM_COST_GROUP=SOC

I2C Connections - SMC			
 Apple Inc.	051-08012	PLATE	D
	4.0.0	REVISION	
	evt-1	STAGE	
	131 OF 700	PAGE	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE RECIPIENT AGREES TO THE FOLLOWING: 1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2. NOT TO REPRODUCE OR COPY IT 3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4. ALL RIGHTS RESERVED			
57 OF 159			

SMC_I2C3

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	3	100kHz	0X4C	0X98	Palm Secure Temp

CHECK SPEED VALUE

SMC_I2C4

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	4	100kHz	0X48	0X90	Temp Sensors

CHECK SPEED VALUE

AOP_I2C0

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AOP	0	400kHz	0X24	0X52	ALS
AOP	0	400kHz	0X24	0X48	ALS Temp

ISP_I2C2

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
ISP	2	400kHz	0X10	0X20	FRONT
ISP	2	400kHz	0X6C	0XD8	Camera Sensor

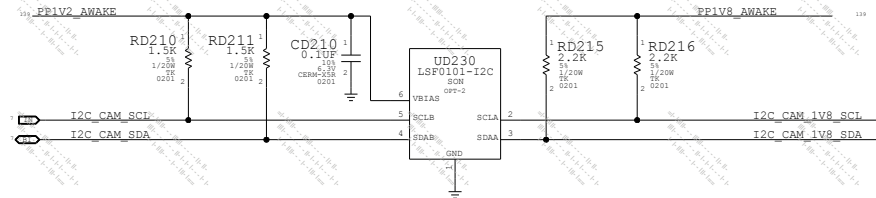
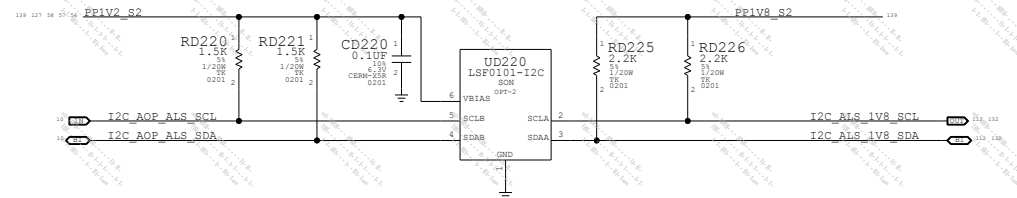
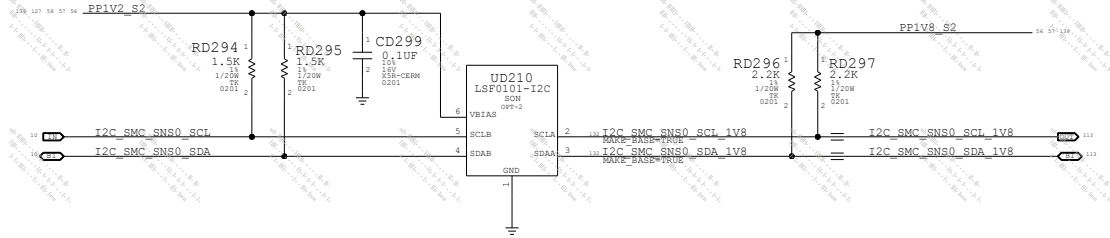
UNUSED and already aliased
ISP_I2C0 SMC_I2C6
ISP_I2C1
ISP_I2C3
AOP_I2C1

SI2C

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
S	0	400kHz	0XXX	0XX	SEP REPRON

Need to confirm if this needs/has pull-ups

MISSING WLAN/BT, R1, CELL - VENDOR CARDS

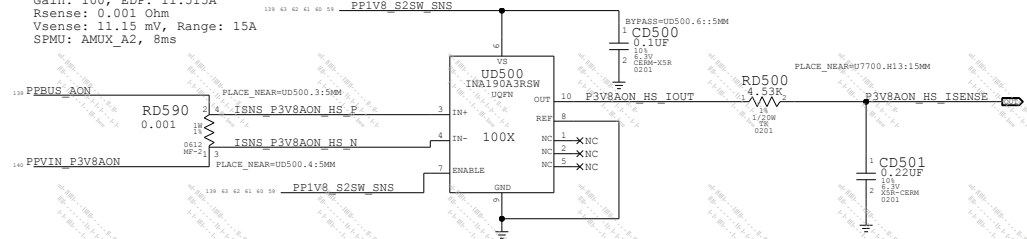


I2C Connections - Other			
Apple Inc.	051-08012	Page	D
	4.0.0	Revision	
NOTICE OF PROPRIETARY PROPERTY:		Branch	evt-1
THE INFORMATION CONTAINED HEREIN IS THE		Page	132 OF 700
PROPRIETARY PROPERTY OF APPLE INC.		Sheet	58 OF 159
ONE SHOULD AGREE TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
I NOT TO REPRODUCE OR COPY IT			
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
I TO ALL RIGHTS RESERVED			

BOM_COST_GROUP=SOC

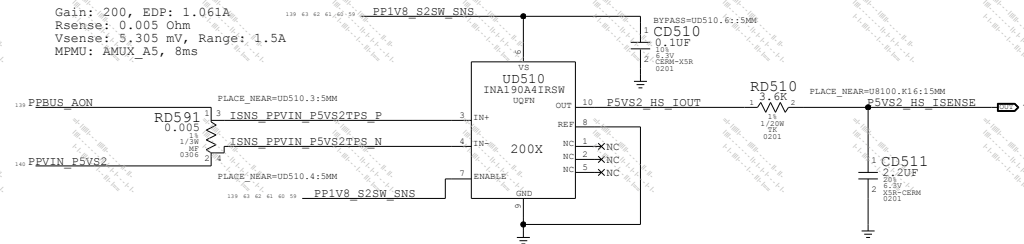
P3V8 AON HIGH SIDE ISENSE (IMVR)

Gain: 100, EDP: 11.515A
Rsense: 0.001 Ohm
Vsense: 11.15 mV, Range: 15A
SPMU: AMUX_A2, 8ms



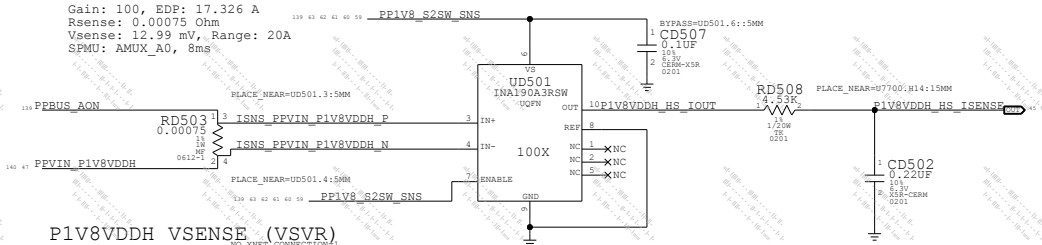
5V S2 VR HIGH SIDE ISENSE (I5SR)

Gain: 200, EDP: 1.061A
Rsense: 0.005 Ohm
Vsense: 5.305 mV, Range: 1.5A
MPMU: AMUX_A5, 8ms



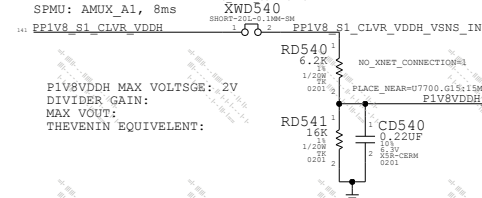
P1V8VDDH HIGH SIDE ISENSE (ISVR)

Gain: 100, EDP: 17.326 A
Rsense: 0.00075 Ohm
Vsense: 12.99 mV, Range: 20A
SPMU: AMUX_A0, 8ms



P1V8VDDH VSENSE (VSVR)

SPMU: AMUX_A1, 8ms

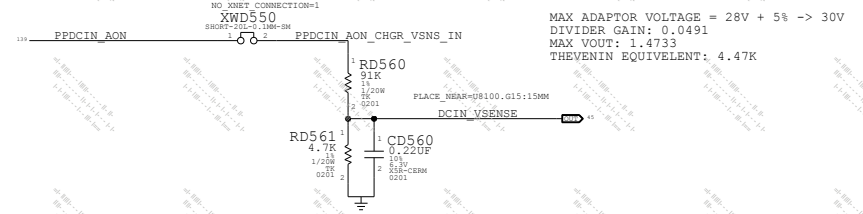


P3V8AON VSENSE

SPMU: AMUX_A2, 8ms
REMOVED in J414c

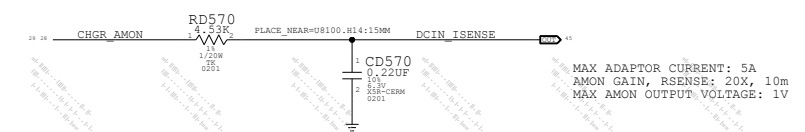
DCIN VOLTAGE SENSE (VD0R)

MPMU: AMUX_A0, 1ms



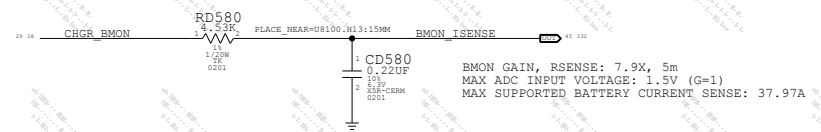
DCIN ISENSE AMON (ID0R)

MPMU: AMUX_A1, 1ms



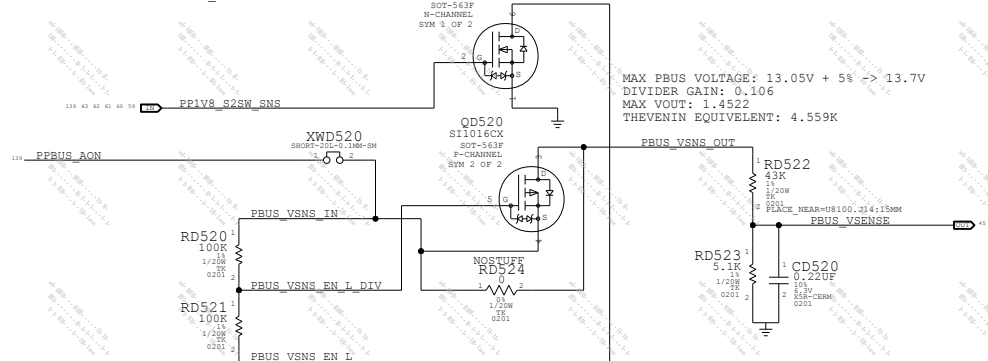
BATTERY ISENSE BMON (IPBR)

MPMU: AMUX_A2, 1ms



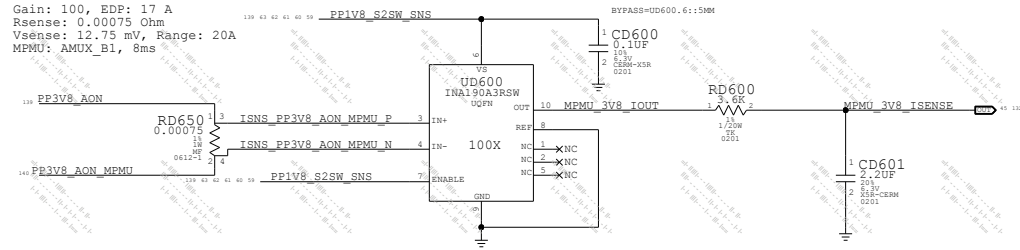
PBUS VOLTAGE SENSE (VP0R)

MPMU: AMUX_A3, 1ms

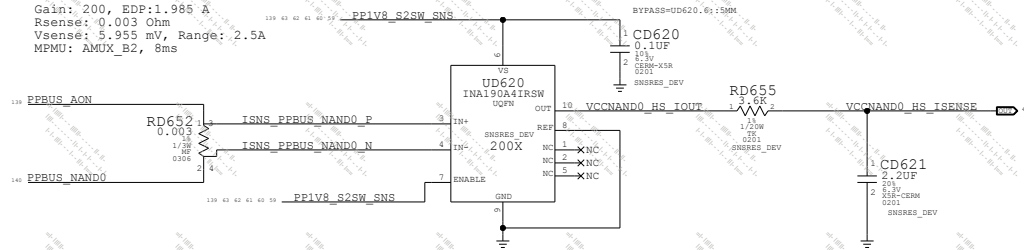


PAGE TITLE			
SENSORS: HIGH-SIDE (1/3)			
 Apple Inc.	051-08012	REV	D
	4.0.0	REVISION	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE			
PROPERTY OF APPLE INC. AND IS NOT			
TO BE REPRODUCED OR COPIED IN ANY			
MANNER WITHOUT THE WRITTEN PERMISSION			
OF APPLE INC.			
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
11 NOT TO REPRODUCE OR COPIY IT			
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
1111 ALL RIGHTS RESERVED			
BOM_COST_GROUP=SENSORS			59 OF 159

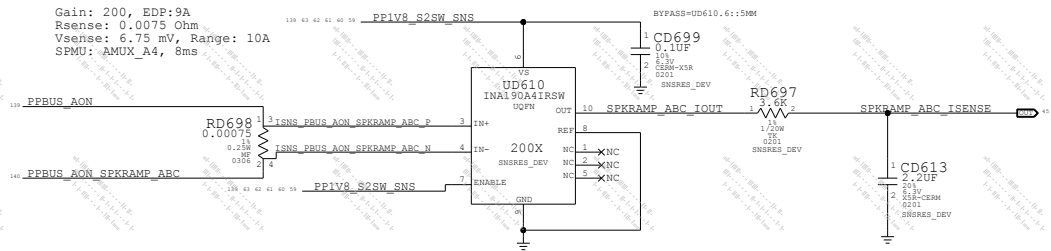
```
Gain: 100, EDP: 17 A
Rsense: 0.00075 Ohm
Vsense: 12.75 mV, Range: 20A
MPMU: AMUX_B1, 8ms
```



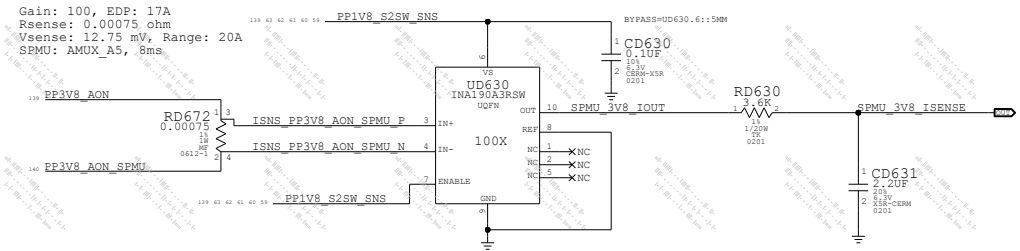
```
Gain: 200, EDP:1.985 A
Rsense: 0.003 Ohm
Vsense: 5.955 mV, Range: 2.5A
MPMU: AMUX_B2, 8ms
```



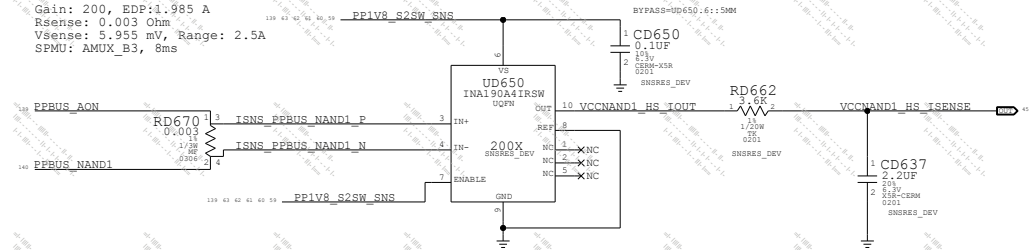
```
Gain: 200, EDP:9A
Rsense: 0.0075 Ohm
Vsense: 6.75 mV, Range: 10A
SPMU: AMUX_A4, 8ms
```



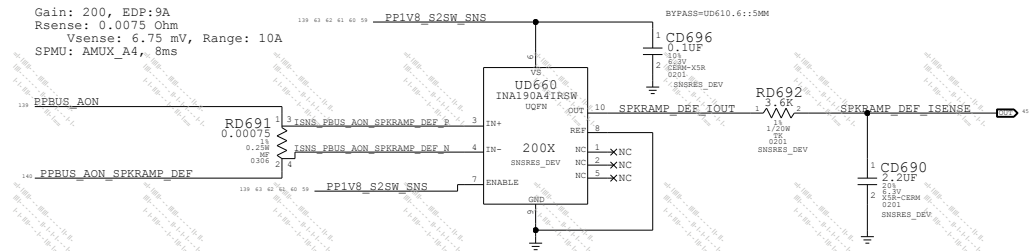
```
Gain: 100, EDP: 17A
Rsense: 0.00075 ohm
Vsense: 12.75 mV, Range: 20A
SPMU: AMUX_A5, 8ms
```

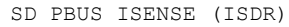


```
Gain: 200, EDP:1.985 A
Rsense: 0.003 Ohm
Vsense: 5.955 mV, Range: 2.5A
SPMU: AMUX_B3, 8ms
```

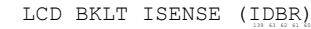
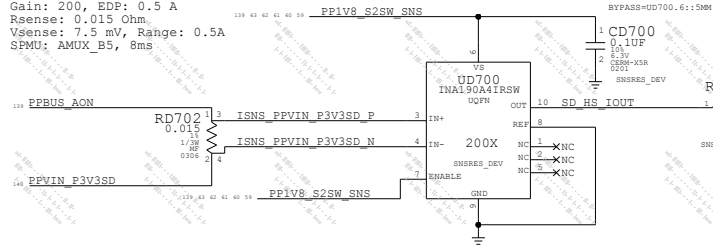


```
Gain: 200, EDP:9A
Rsense: 0.0075 Ohm
Vsense: 6.75 mV, Range: 10A
SPMU: AMUX_A4, 8ms
```

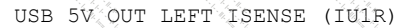
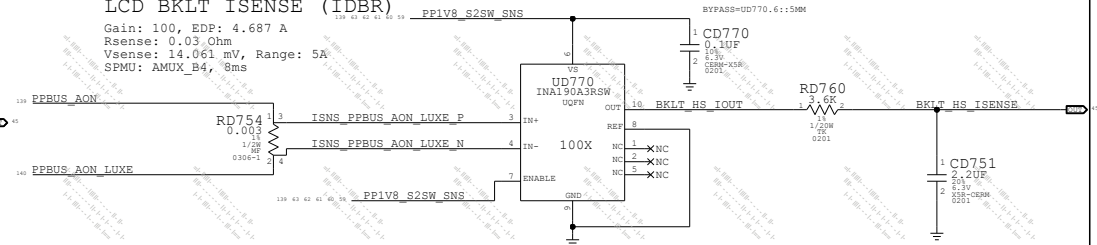




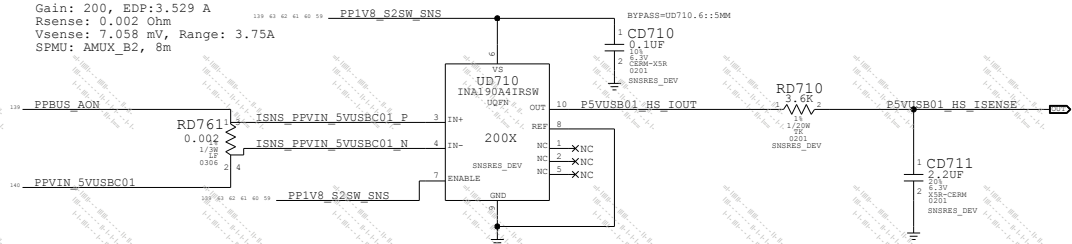
```
Gain: 200, EDP: 0.5 A
Rsense: 0.015 Ohm
Vsense: 7.5 mV, Range: 0.5A
SPMU: AMUX_B5, 8ms
```



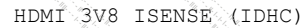
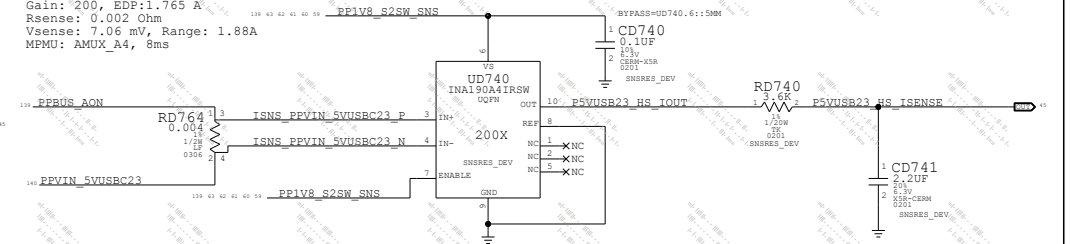
```
Gain: 100, EDP: 4.687 A
Rsense: 0.03 Ohm
Vsense: 14.061 mV, Range: 5A
SPMU: AMUX_B4, 8ms
```



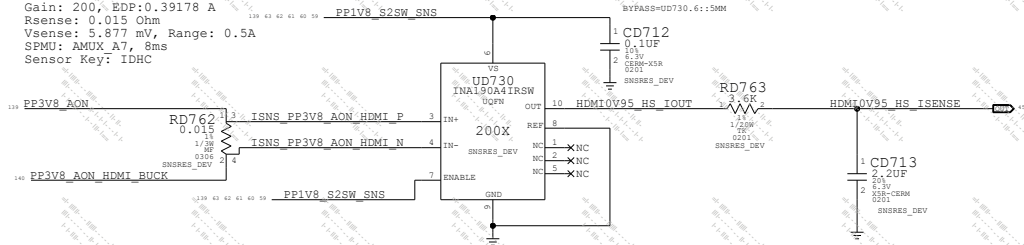
```
Gain: 200, EDP:3.529 A
Rsense: 0.002 Ohm
Vsense: 7.058 mV, Range: 3.75A
SPMU: AMUX_B2, 8m
```

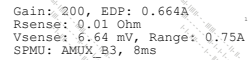
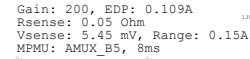
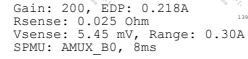
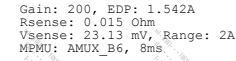
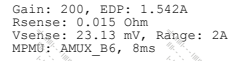


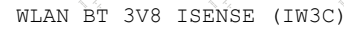
```
Gain: 200, EDP:1.765 A
Rsense: 0.002 Ohm
Vsense: 7.06 mV, Range: 1.88A
MPMU: AMUX_A4, 8ms
```



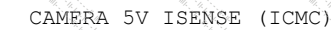
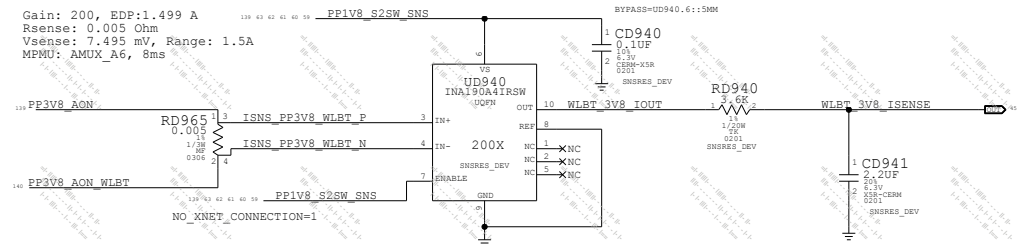
```
Gain: 200, EDP:0.39178 A
Rsense: 0.015 Ohm
Vsense: 5.877 mV, Range: 0.5A
SPMU: AMUX_A7, 8ms
Sensor Key: IDHC
```



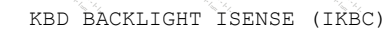
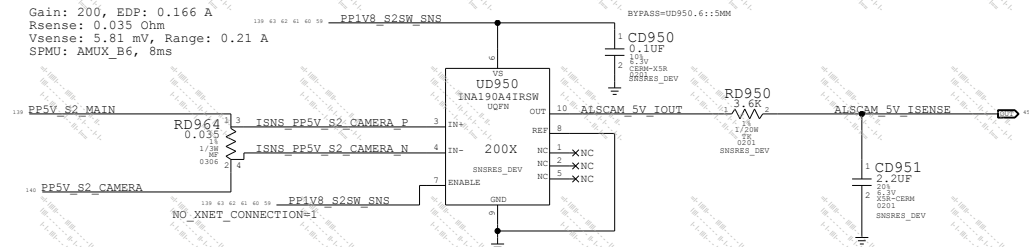




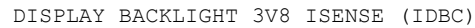
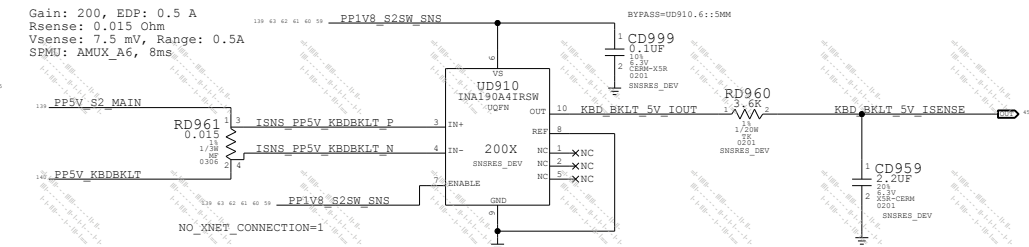
Gain: 200, EDP:1.499 A
Rsense: 0.005 Ohm
Vsense: 7.495 mV, Range
MPMU: AMUX_A6, 8ms



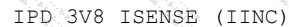
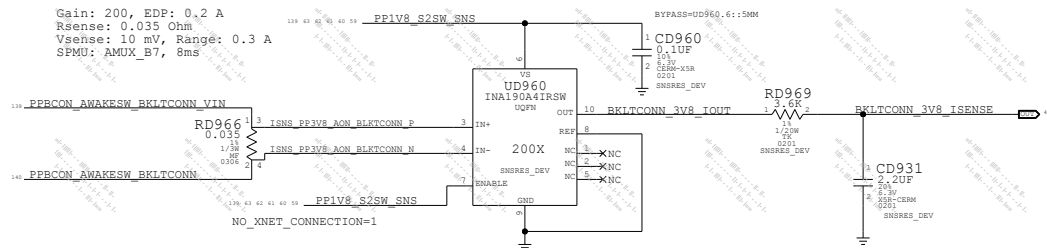
```
Gain: 200, EDP: 0.166 A
Rsense: 0.035 Ohm
Vsense: 5.81 mV, Range: 0.21 A
SPMU: AMUX_B6, 8ms
```



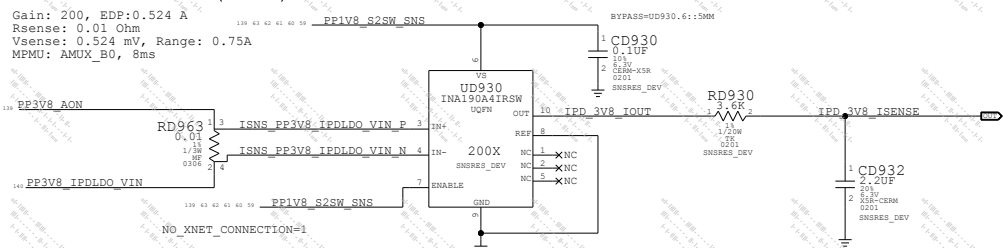
```
Gain: 200, EDP: 0.5 A
Rsense: 0.015 Ohm
Vsense: 7.5 mV, Range: 0.5A
SPMU: AMUX A6, 8ms
```



```
Gain: 200, EDP: 0.2 A
Rsense: 0.035 Ohm
Vsense: 10 mV, Range: 0.3 A
SPMU: AMUX_B7, 8ms
```



```
Gain: 200, EDP:0.524 A
Rsense: 0.01 Ohm
Vsense: 0.524 mV, Range: 0.75A
MPMU: AMUX B0, 8ms
```



P1V8VDDH LOW SIDE ISENSE (IMON)
MPMU AMUX_B4, 8ms, VMAX AFTER DIVIDER = 1.51V

REMOVED per J416 James released 0.34.3

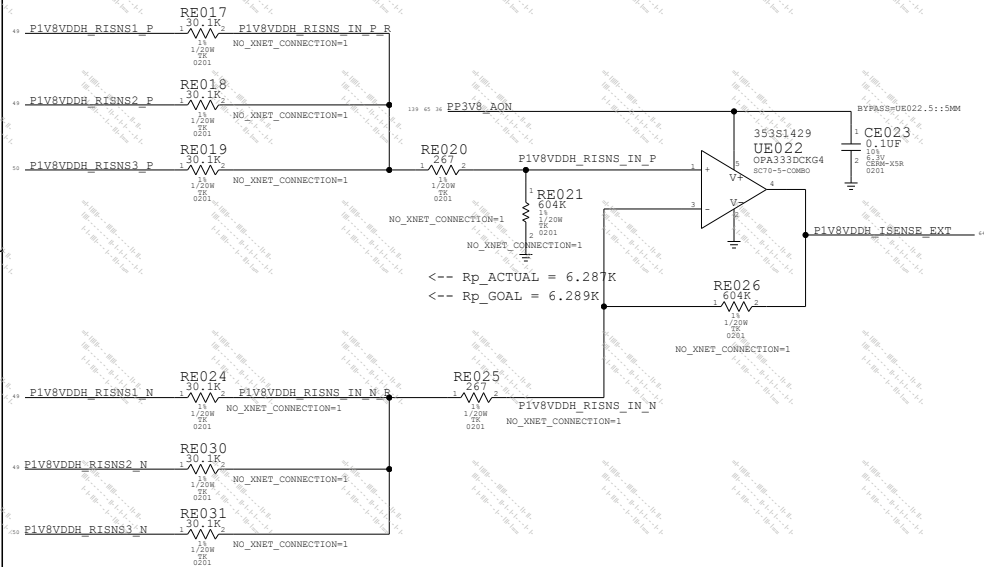
P3V8 LOW SIDE ISENSE (IMON)
SPMU AMUX_A7, 8ms, VMAX AFTER DIVIDER = 1.51V

P1V8VDDH LOW SIDE ISENSE (SUMMING AMP FOR 5 PHASES)

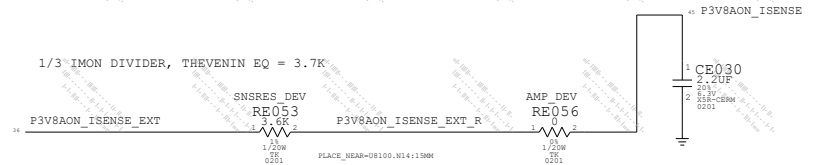
EDP: 156.2A, 32.24A/PHASE

SPMU AMUX_A7, 8ms

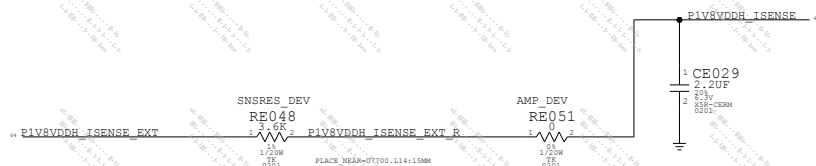
[[P3V8 LOW SIDE ISENSE AND ILIMIT moved to CSA60]]



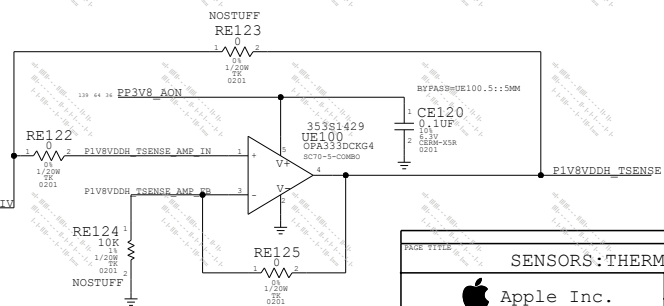
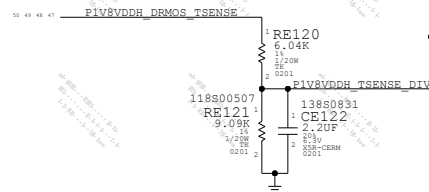
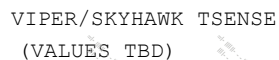
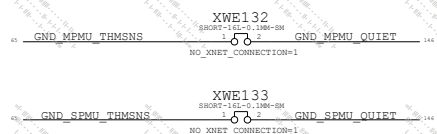
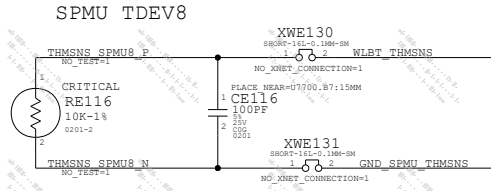
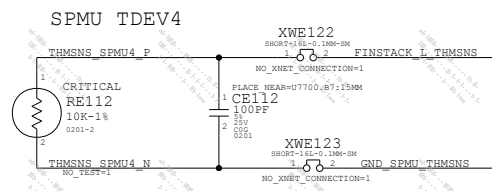
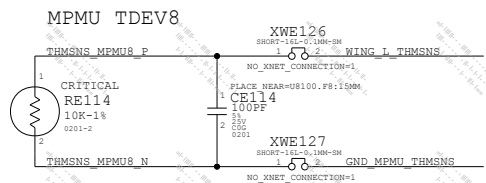
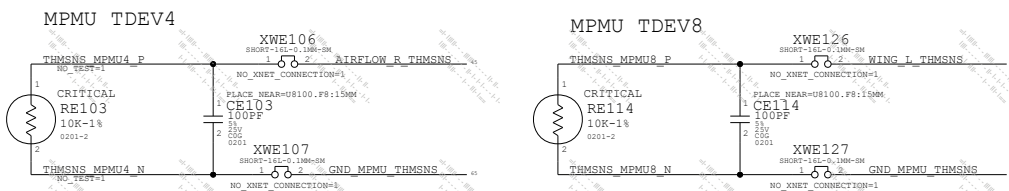
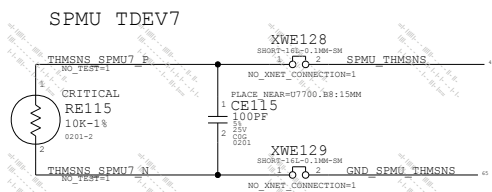
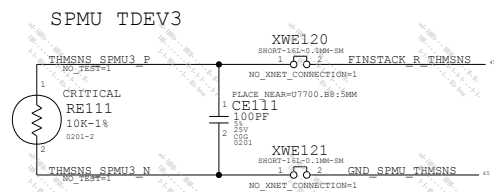
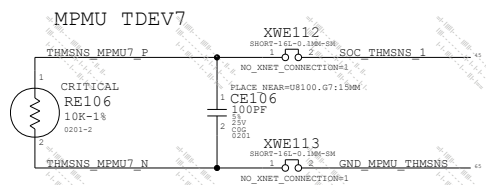
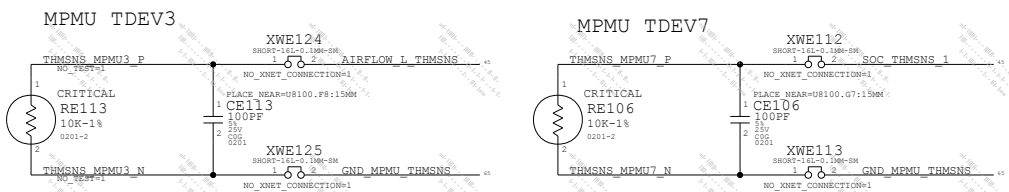
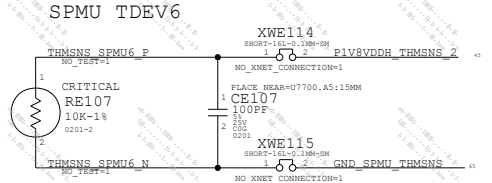
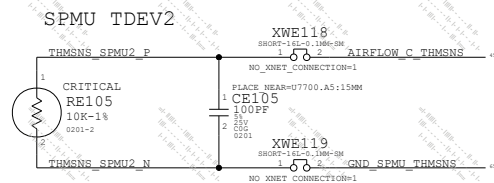
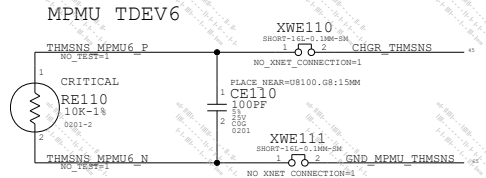
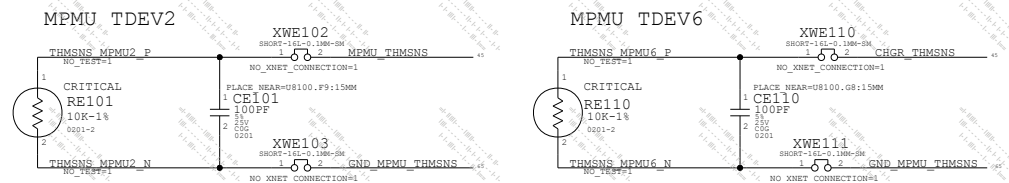
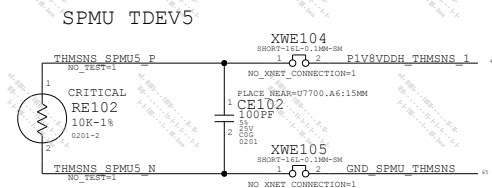
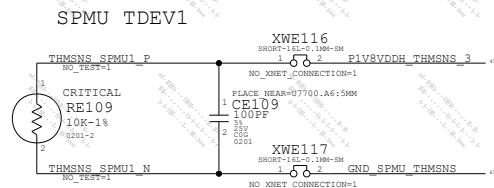
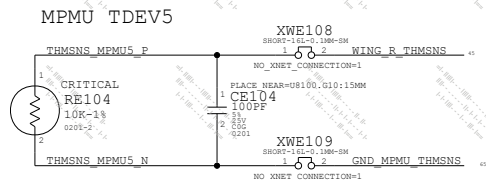
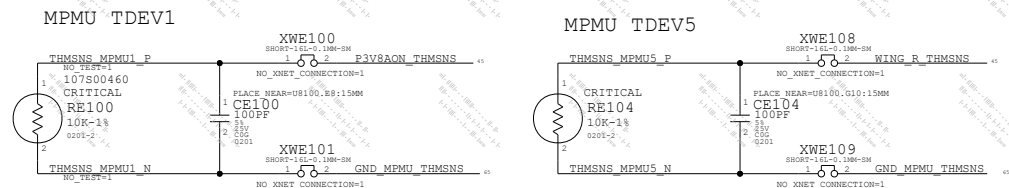
RESISTOR STUFFING SUMMING AMP



RESISTOR STUFFING OPTION FOR IMON OR SUMMING AMP



PAGE TITLE: SENSORS: LOW-SIDE (3/3)			
	REVISION	051-08012	PAGE D
	REVISION	4.0.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE REVISIONS AGREE TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED			
BOM_COST_GROUP=SENSORS			140 OF 700
			64 OF 159



PAGE TITLE		SENSORS: THERMAL	
 Apple Inc.	ORIGINATOR NUMBER	051-08012	DISPOSITION
	4.0.0		
	BRANCH	evt-1	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE FOLLOWING APPLIES TO ALL INFORMATION:		PAGE	141 OF 700
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2. NOT TO REPRODUCE OR COPY IT 3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IN ANY MANNER RESERVED		SERIES	65 OF 159

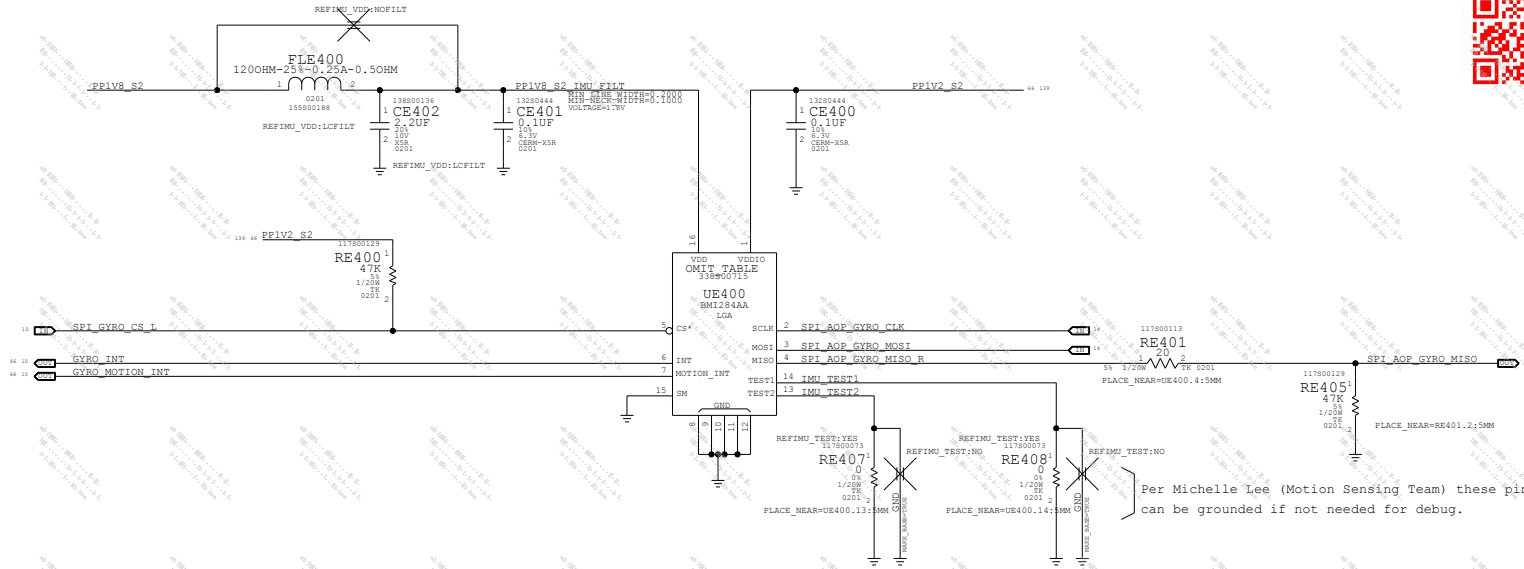
BOM_COST_GROUP=SENSORS

A Sovereign Accelerometer and Gyroscope

Datasheet Radar:



*** OK2INTEGRATE ***



MFG: Bosch
MPN: BMI284AA
APN: 338S00715
URL: <https://www.bosch-sensortec.com/products/motion-sensors/imus/>
Radar: <https://61521702> (Sovereign: Datasheet)

B Test Points

TPE400 PACK_OPTION=REFIMU_TP:P5MM
A GYRO_INT 10 44
TP-F5
998-4756

TPE401 PACK_OPTION=REFIMU_TP:P5MM
A GYRO_MOTION_INT 10 44
TP-F5
998-4756

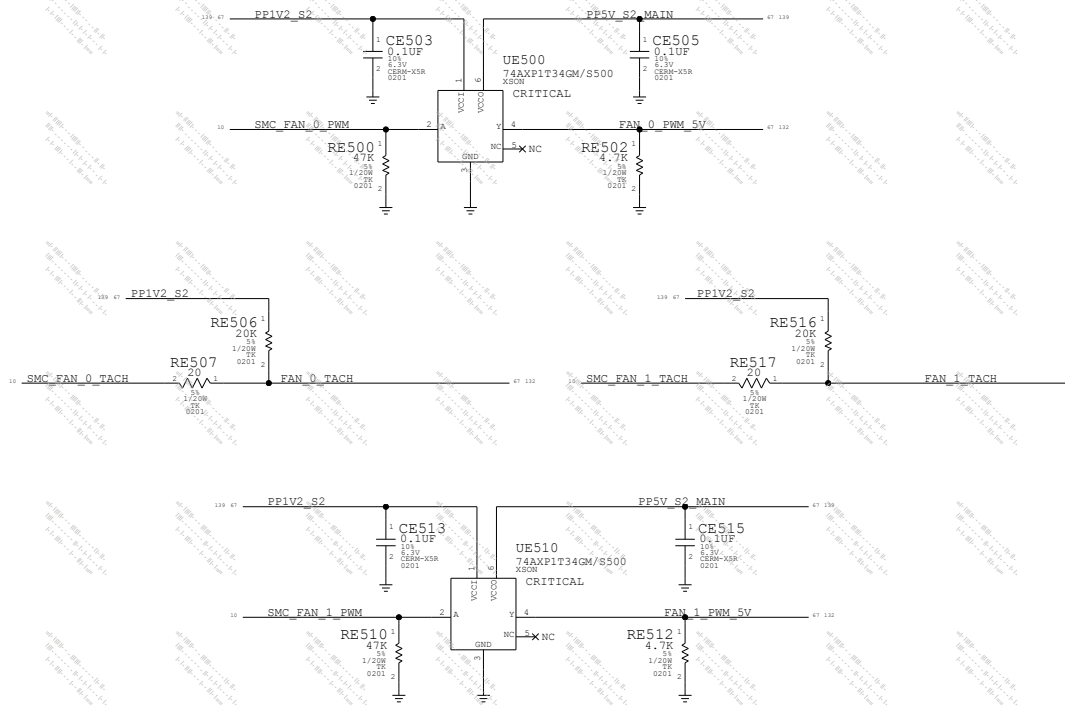
C Sovereign BOM Options

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00715	1	IC, SOVEREIGN, BMI284, AA, LGA16	UE400	CRITICAL	REFIMU_IC: BMI284
338S00849	1	IC, SOVEREIGN, BMI286, AA, LGA16	UE400	CRITICAL	REFIMU_IC: BMI286

SENSORS: MOTION		
 Apple Inc.	REVISION	051-08012
	4.0.0	
NOTICE OF PROPRIETARY PROPERTY:		144 OF 700
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE EXPRESS WRITTEN PERMISSION OF APPLE INC.		66 OF 159

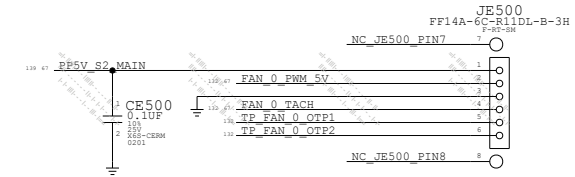
FAN CONTROLLERS

FAN PWM LEVEL SHIFTER

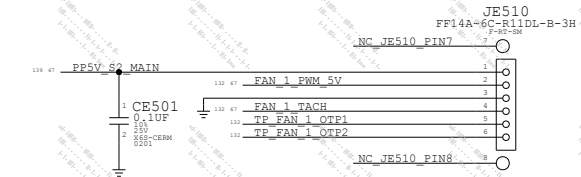


*DUMMY FAN TO PLUG INTO EITHER POR FAN CONNECTORS JE500 OR JE510

PWM FAN0 (LEFT) CONNECTOR



PWM FAN1 (RIGHT) CONNECTOR



PAGE TITLE			
FANS			
Apple Inc.	051-08012	DATE	D
	4.0.0	REVISION	
NOTICE OF PROPRIETARY PROPERTY:			evt-1
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE REVISIONS ARE OF THE FOLLOWING:			145 OF 700
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			67 OF 159
I NOT TO REPRODUCE OR COPY IT			
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
I TO ALL RIGHTS RESERVED			

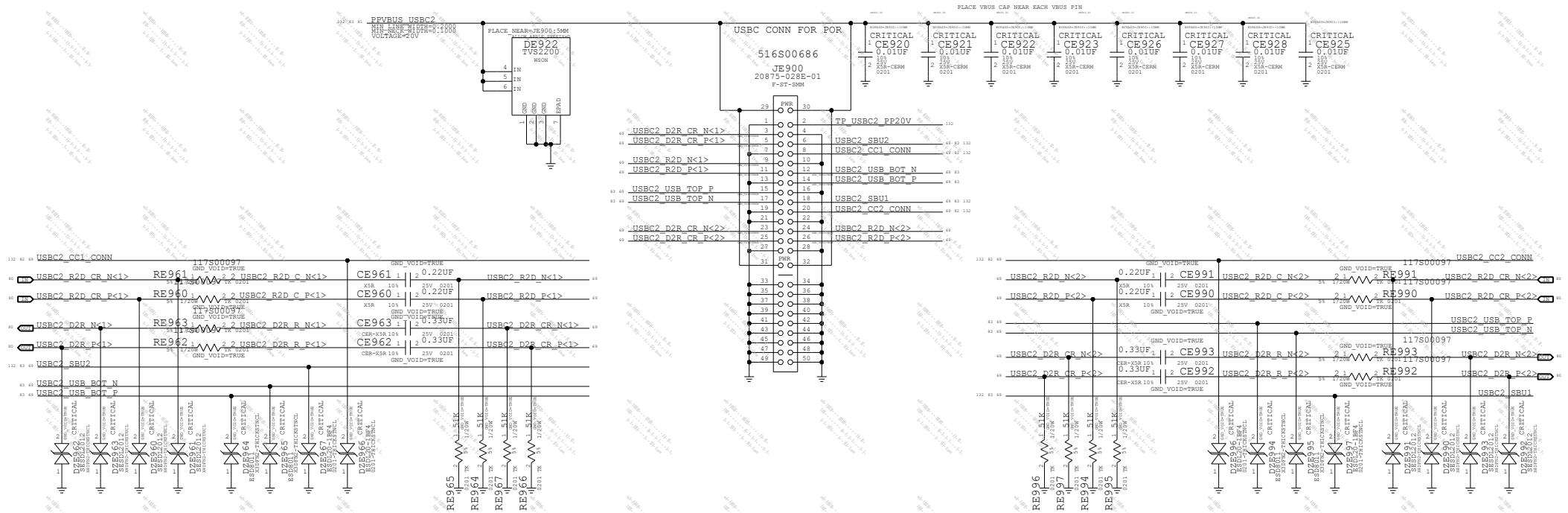
BOM_COST_GROUP=FANS

D

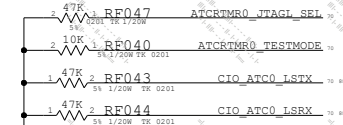
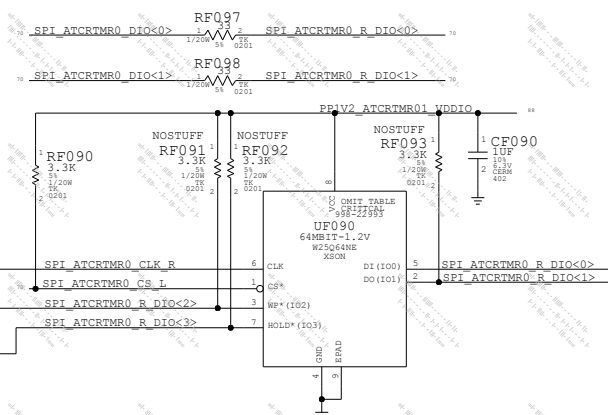
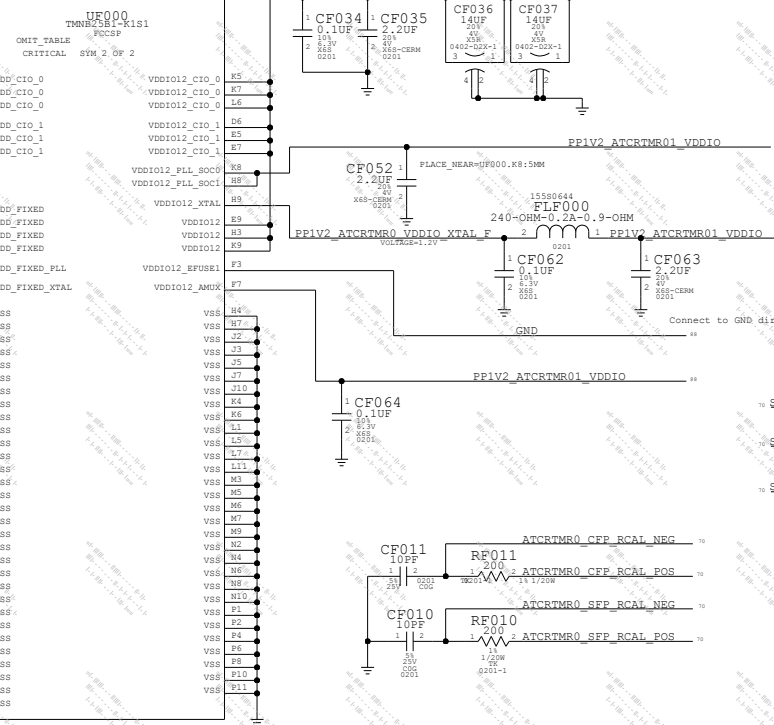
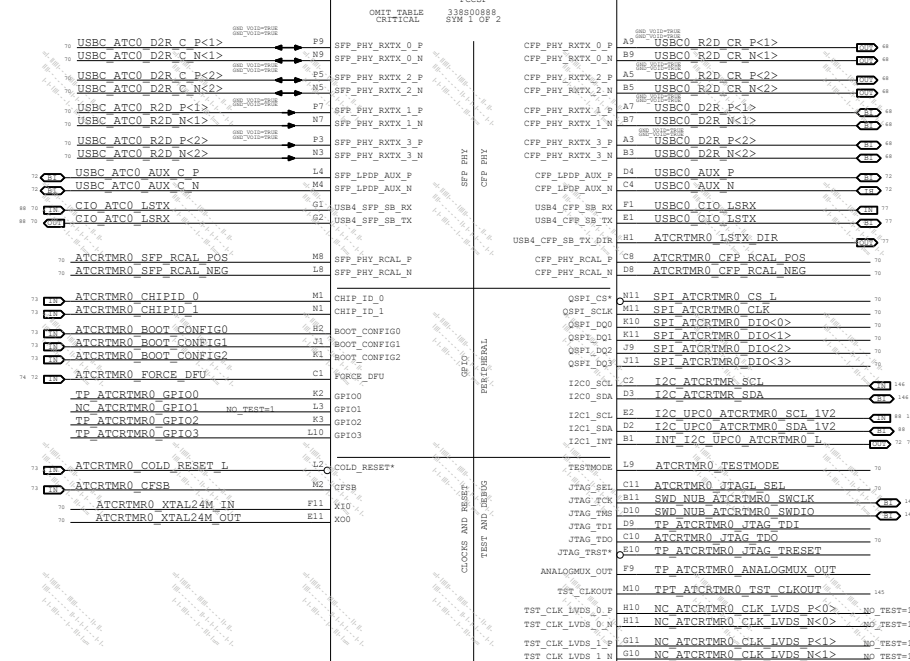
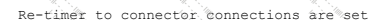


BOM_COST_GROUP=USB-C

Right Side Port



PAGE TITLE			
USB-C: Right Connector			
 Apple Inc.	DATE	051-08012	D
	REVISION	4.0.0	
	DESCRIPTION	cvt-1	
	PRICE	149 OF 700	
	69 OF 159		



USB-C • High Speed ATC0

 Apple Inc.

PROPERTY PROPERTY

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.

THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

2	
---	--

2	
---	--

DRAWING NUMBER	051 00012
----------------	-----------

031-08012
REVISION

4.0.0

BRANCH

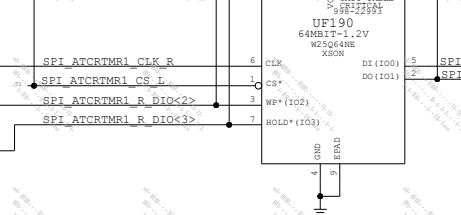
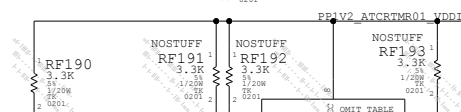
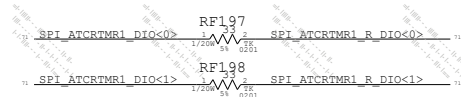
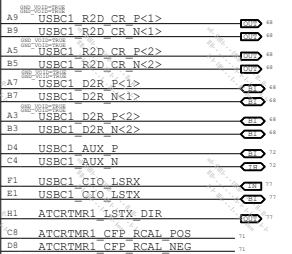
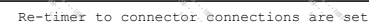
evl-1

150 OF 70

70 OF 150

70	GE% 15:
----	---------

1



PAGE NUMBER 001 OF 001		DATE 08/08/2012	
TITLE			
USB-C: High Speed ATC1			
 Apple Inc.		0511-08012	D
		REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. FOR YOUR INFORMATION, THE FOLLOWING AGREE TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		BRANCH	evt-1
I NOT TO REPRODUCE OR COPY IT		PAGE	151 OF 700
I NOT TO FURNISH OR PUBLISH IT IN WHOLE OR PART		NUMBER	71 OF 159

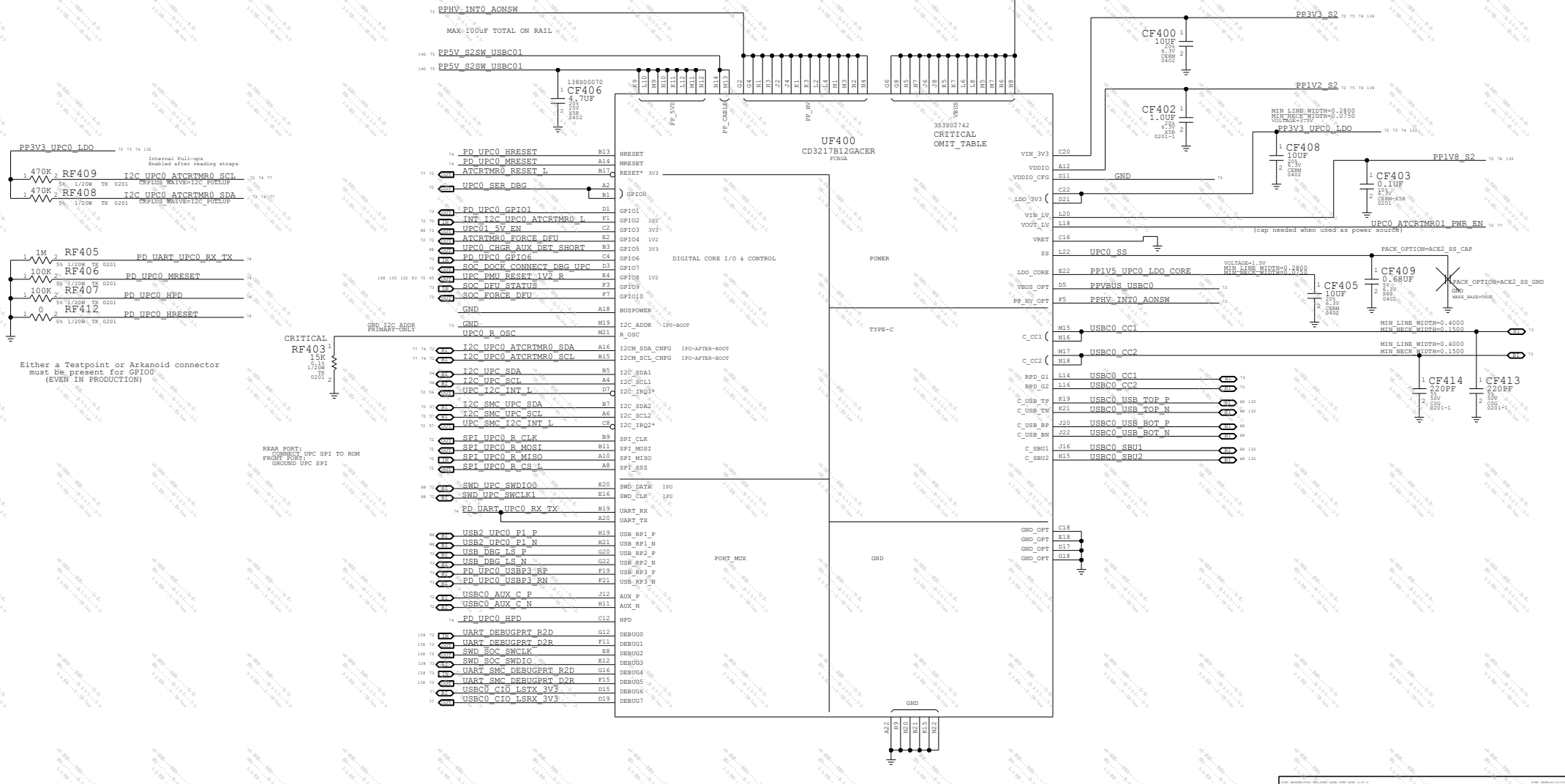
*** OK2PLACE ***

D

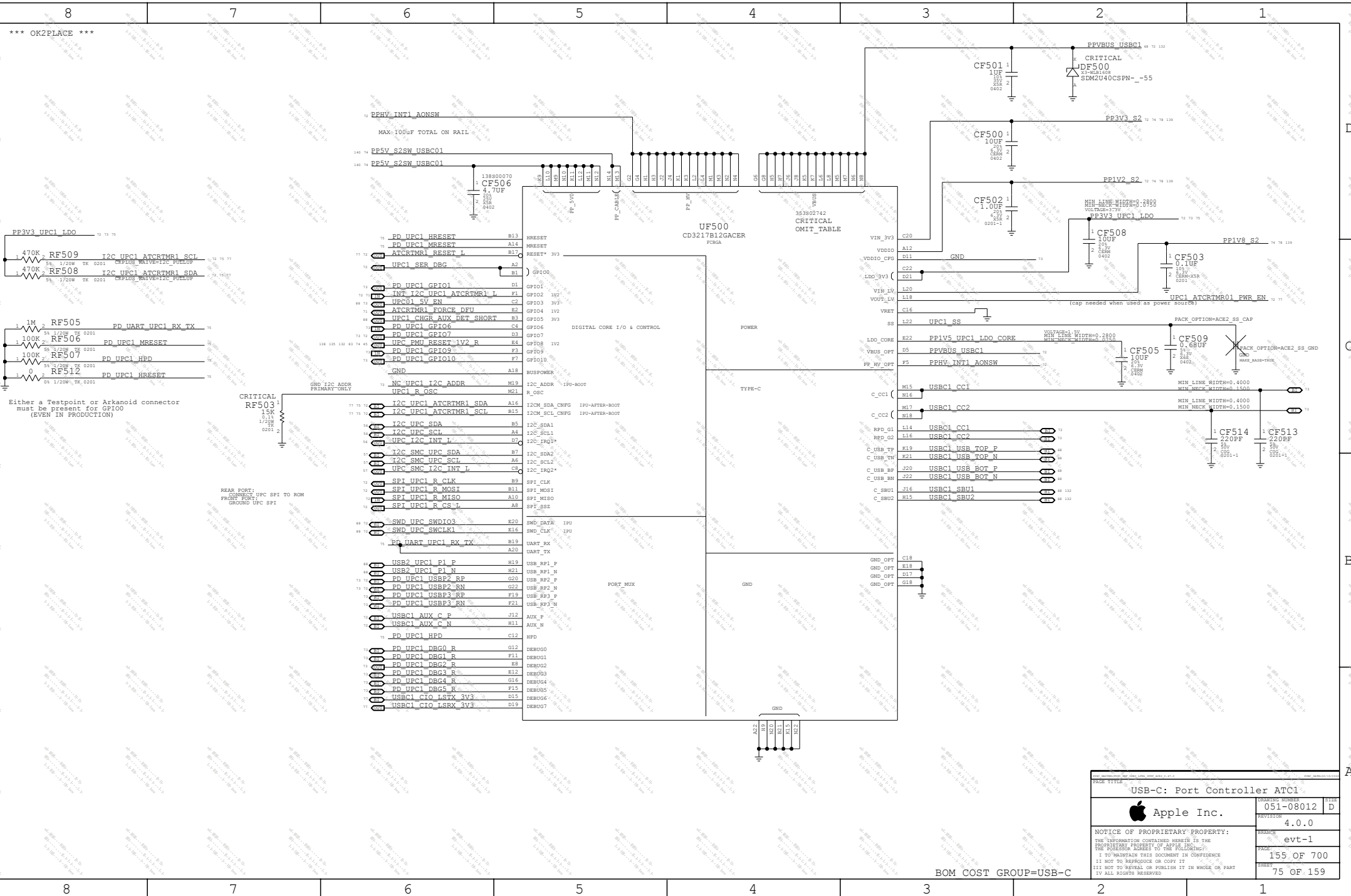
C

B

A



PAGE TITLE			
USB-C: Port Controller ATC0			
Apple Inc.	REVISION	051-08012	PAGE D
	4.0.0		
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
11 NOT TO REPRODUCE OR COPY IT			
11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
11 ALL RIGHTS RESERVED			
154 OF 700			74 OF 159



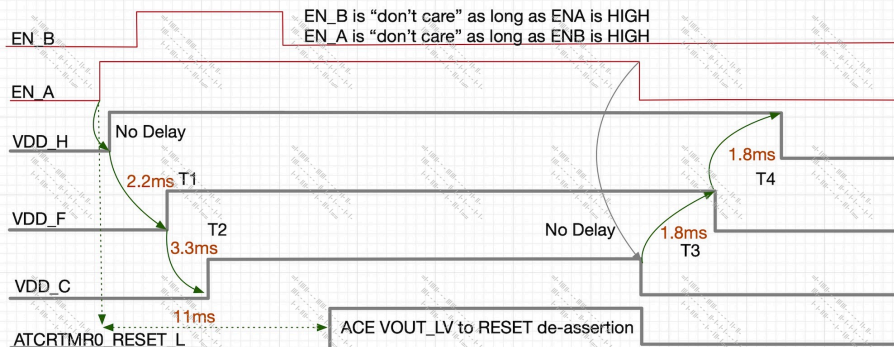
Sequencing Requirements: 3.3V to UF790 --> system 1.2V (UF710,UF720) same time or before system 1.8V (UF400&UF500 VIN_LV pin)

ATC0 RE-TIMER I2C LEVEL SHIFTERS

ATC1 RE-TIMER I2C LEVEL SHIFTERS

ATC0/1 AND MACAE RESET LEVEL SHIFTERS

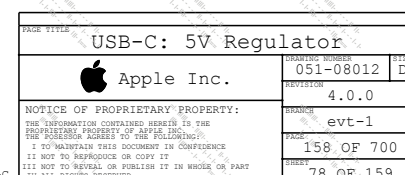
Note1: As long as EN_A or EN_B are HIGH, the outputs stay HIGH
Note2: Outputs are an Ored and delayed version of EN_A or EN_B



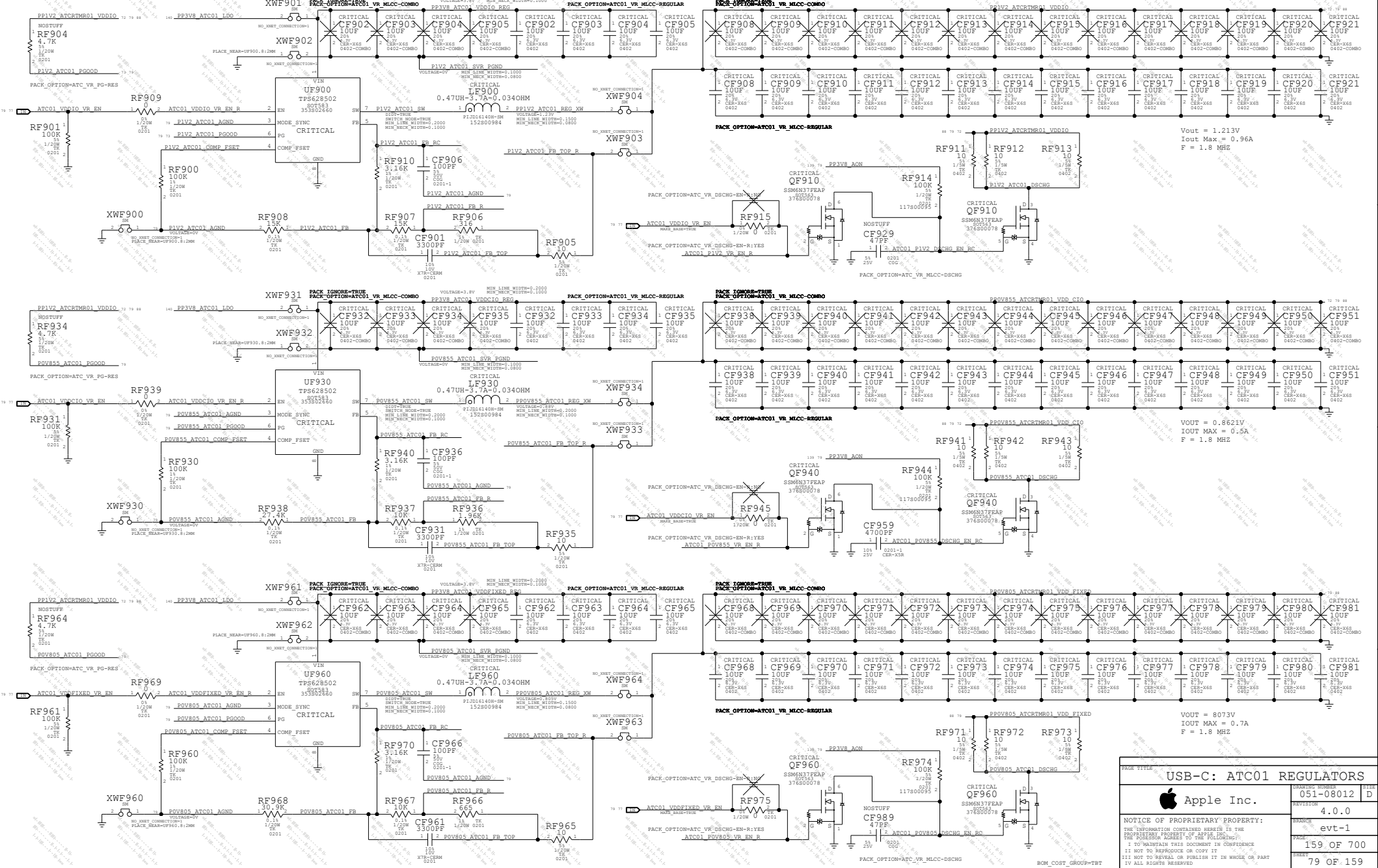
USB-C: HS Level Shifters ATC01

Apple Inc.	051-08012	D
NOTICE OF PROPRIETARY PROPERTY:	4.0.0	
THE INFORMATION CONTAINED HEREIN IS THE	evt-1	
PROPRIETARY PROPERTY OF APPLE INC.	157 OF 700	
THE INFORMATION CONTAINED HEREIN IS NOT	77 OF 159	
TO BE REPRODUCED OR COPIED IN ANY FORM		
WITHOUT THE EXPRESS WRITTEN PERMISSION		
OF APPLE INC.		

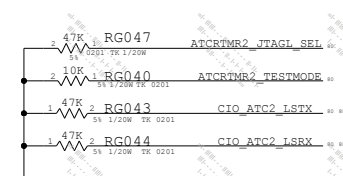
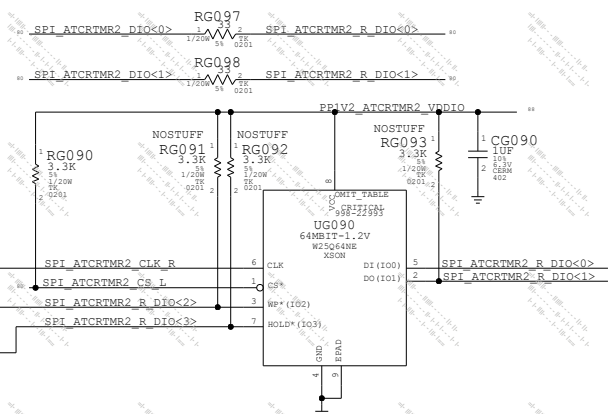
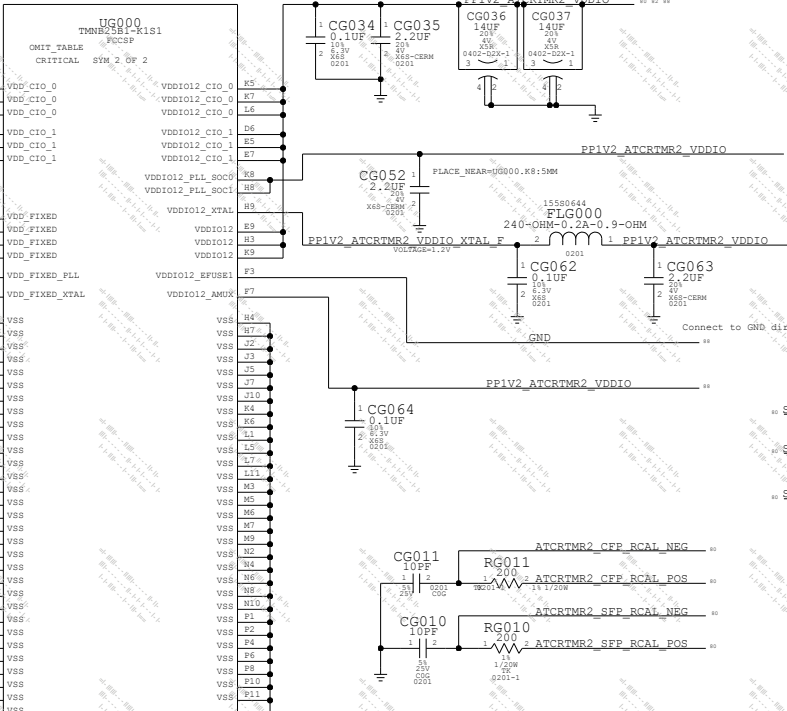
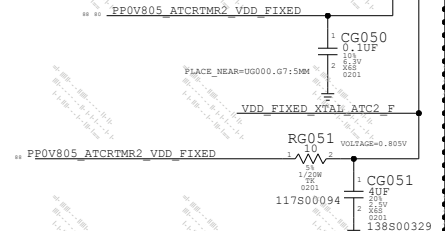
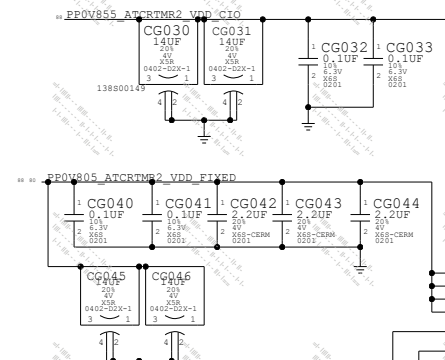
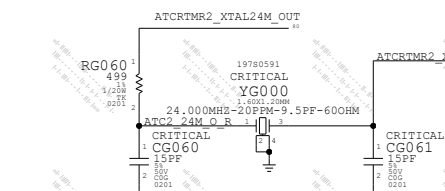
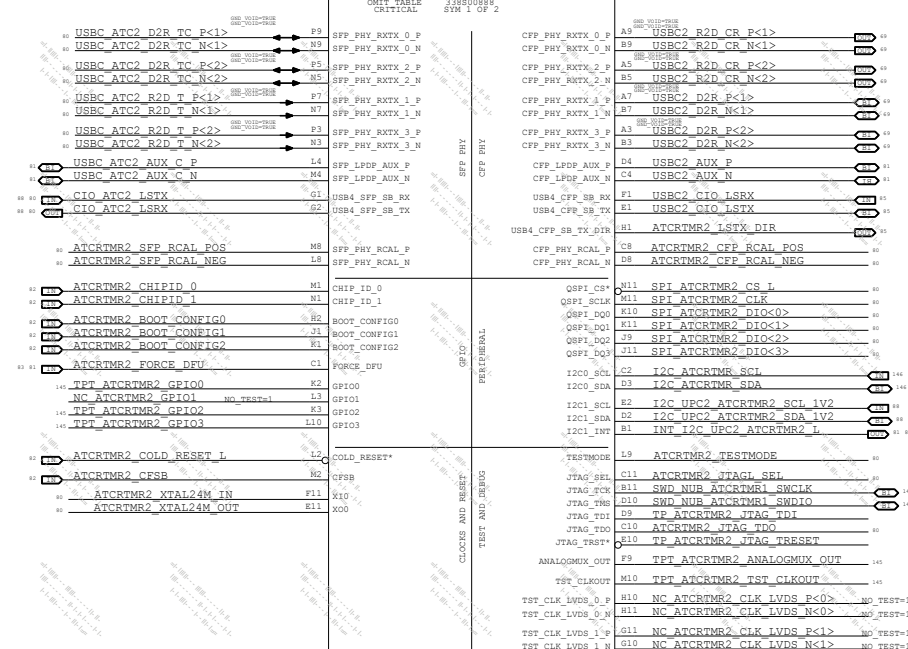
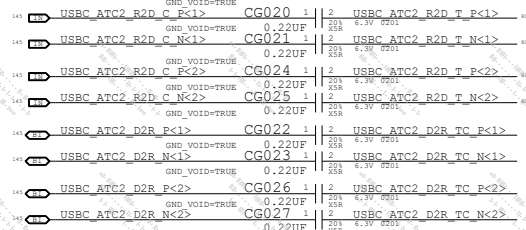
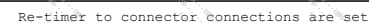
```
SET ONE OPTION FOR UF840 BUFFER
PACK_OPTION=5VUSBC01_AND:PP
PACK_OPTION=5VUSBC01_AND:OD
```



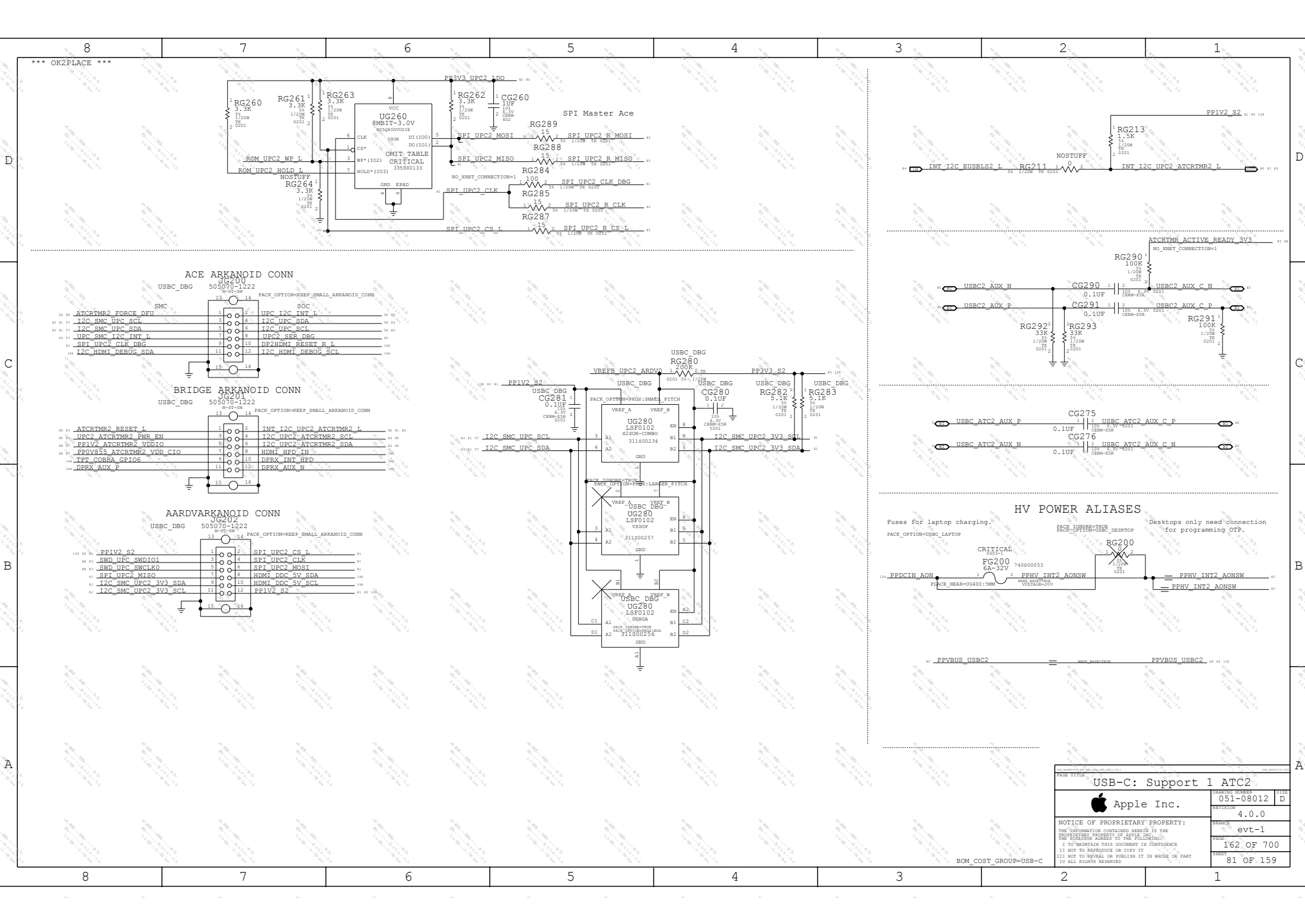
*** OK2INTEGRATE ***



PAGE TITLE			
USB-C: ATC01 REGULATORS			
Apple Inc.		051-08012	D
NOTICE OF PROPRIETARY PROPERTY:		4.0.0	
THE INFORMATION CONTAINED HEREIN IS THE		evt-1	
PROPERTY OF APPLE INC.		159 OF 700	
THIS DOCUMENT IS UNCLASSIFIED		79 OF 159	
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
11 NOT TO REPRODUCE OR COPY IT			
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
1V ALL RIGHTS RESERVED			

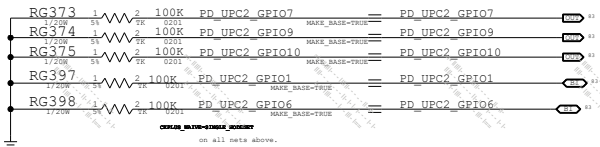
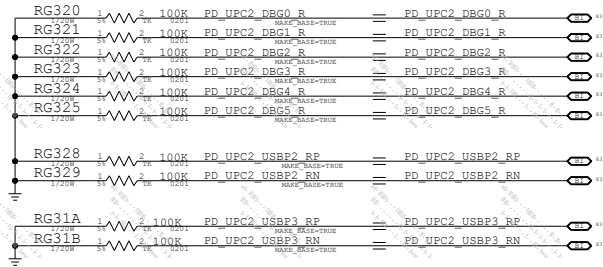


PAGE TITLE		USB-C: High Speed ATC2	
 Apple Inc.	DRAWING NUMBER	051-08012	
	REVISION	4.0.0	
	DESCRIPTION	evt-1	
NOTICE OF PROPRIETARY PROPERTY:		PRICE	160 OF 700
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE FOLLOWING AGREES TO THIS NOTICE:		QUANTITY	80 OF 159
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED			



Ace 2 unused GPIOs and Ports

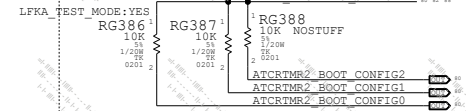
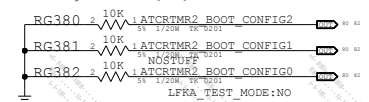
Ace2 GPIOs



on all nets above.

ATCRTMR Boot Config

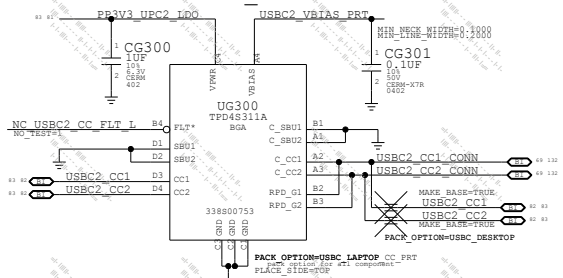
[2:0] = [011] 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabled



ATCRTMR0 CHIP 0X2



USBC0 PP CABLE Protection



ATC0: I2C_ADDR=GND, I2CM * CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC1: I2C_ADDR=Float, I2CM * CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC2: I2C_ADDR=GND, I2CM * CNFG=1M\u03a9 3V3_LDO_X pull-downs
ATC3: I2C_ADDR=Float, I2CM * CNFG=1M\u03a9 3V3_LDO_X pull-downs

OMIT_TABLE

RG351



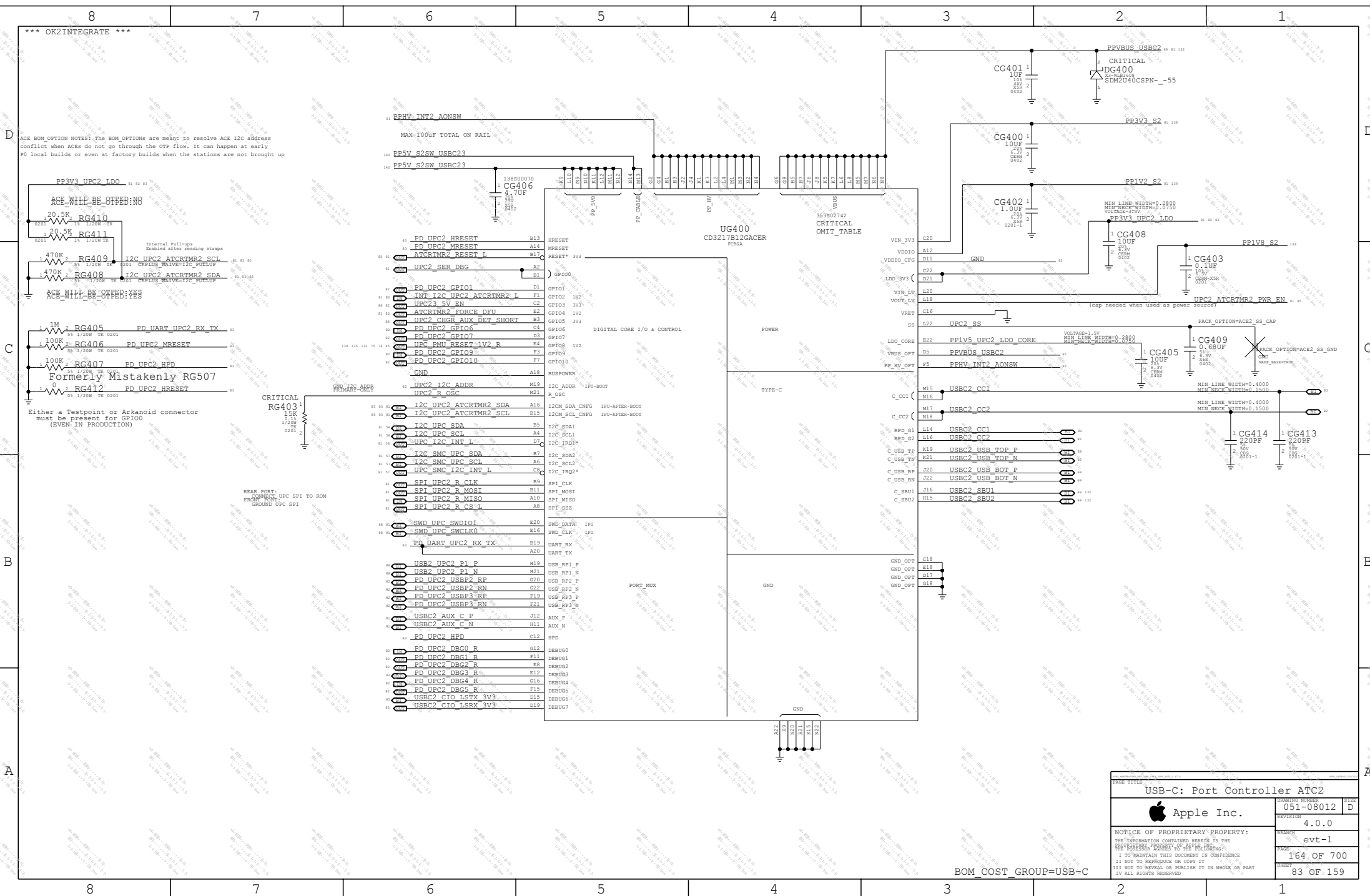
Is UPCx_5V_EN being used?



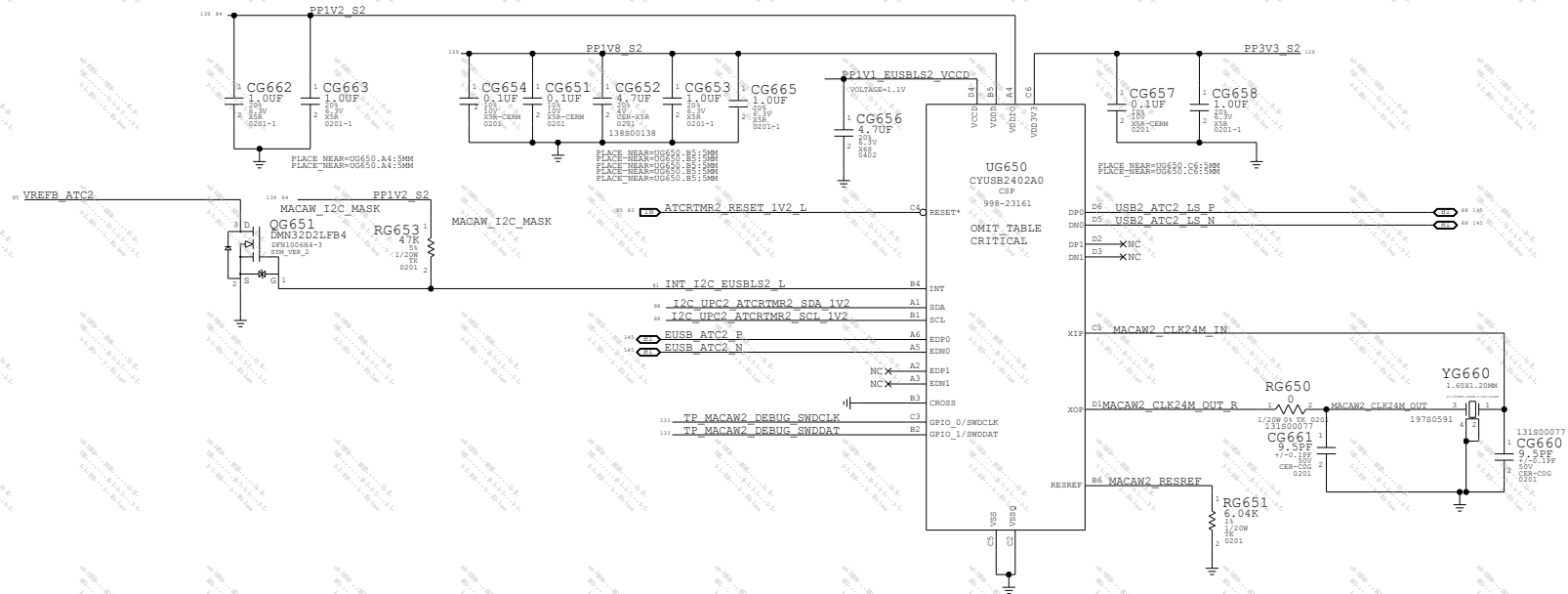
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117800073	1	RES,78,0 OHM,1A MAX,1/20W,0201	RG351	CRITICAL	ACE_WILL_BE_0PTED:YES
118800466	1	RES,78,100OHM,1A,1/20W,0201	RG351	CRITICAL	ACE_WILL_BE_0PTED:NO

PAGE TITLE		PAGE D	
USB-C: Support 2 ATC2		051-08012	
Apple Inc.		4.0.0	
NOTICE OF PROPRIETARY PROPERTY:		evt-1	
THE INFORMATION CONTAINED HEREIN IS THE		163 OF 700	
PROPERTY OF APPLE INC.		82 OF 159	
THE INFORMATION CONTAINED HEREIN IS THE			
PROPERTY OF APPLE INC.			
THE INFORMATION CONTAINED HEREIN IS THE			
PROPERTY OF APPLE INC.			

BOM_COST_GROUP=USB-C

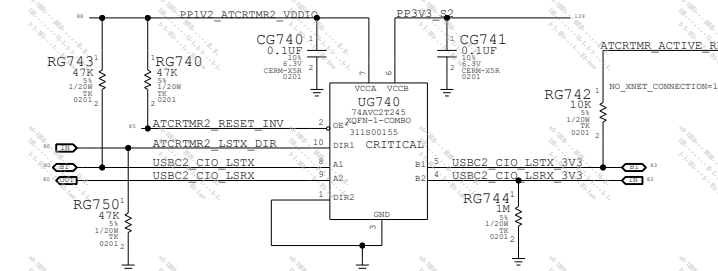


MACAW 2



PAGE TITLE			
USB-C: USB2 RPT2			
 Apple Inc.	CHANGING NUMBER	051-08012	
	REVISION	4.0.0	
	NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE FOLLOWING AGREES TO MAINTAIN THE CONFIDENTIALITY OF THE INFORMATION CONTAINED HEREIN AND TO MAINTAIN THIS DOCUMENT IN CONFIDENCE IT IS NOT TO REPRODUCE OR COPY IT IT IS NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART ALL RIGHTS RESERVED		
BRANCH	evt-1		
PAGE	166 OF 700		
PAGES	84 OF 159		

Sequencing Requirements: 3.3V to UG790 --> system 1.2V (UG710) same time or before system 1.8V (UG400 VIN LV pin)



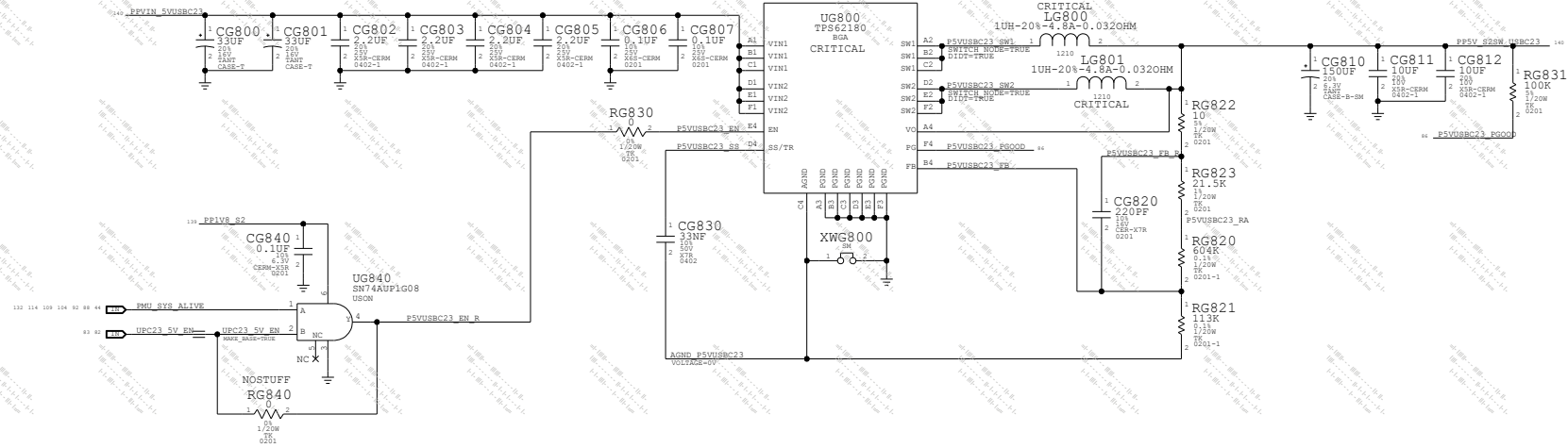
The schematic diagram illustrates the ATCRTMR2 reset circuit in two configurations. In the top configuration, a pull-up resistor (RG755) connects PPIV2_ATCRTMR2_VDDIO to the input of a 31140286 UG730 SN74AUP1G17 inverter. A capacitor (CG730) is connected between the input and the output of the inverter. The output of the inverter is connected to ATCRTMR2_RESET_INV. In the bottom configuration, a pull-up resistor (RG756) connects PPIV2_ATCRTMR2_VDDIO to the input of a 311800286 UG750 SN74AUP1G06 inverter. A capacitor (CG750) is connected between the input and the output of the inverter. The output of the inverter is connected to ATCRTMR2_RESET_INV. Both circuits include a connection to ATCRTMR2_RESET_L.

[illegible]

PAGE 11111111		051-08012		D	
USB-C: HS Level Shifters ATC2		REVISION		4.0.0	
 Apple Inc.		PART		evt-1	
NOTICE OF PROPRIETARY PROPERTY:		PAGE		167 OF 700	
THE INFORMATION CONTAINED HEREIN IS THE		PAGE		85 OF 159	
PROPERTY OF, AND IS LOANED TO, THE FOLLOWING:		PAGE			
1. NOT TO REPRODUCE OR COPY IT		PAGE			
2. NOT TO DISCLOSE OR DISTRIBUTE IT		PAGE			
3. NOT TO REVEAL OR FORNISH IT IN WHOLE OR PART		PAGE			
4. ALL RIGHTS ARE RESERVED		PAGE			

*** OK2INTEGRATE ***

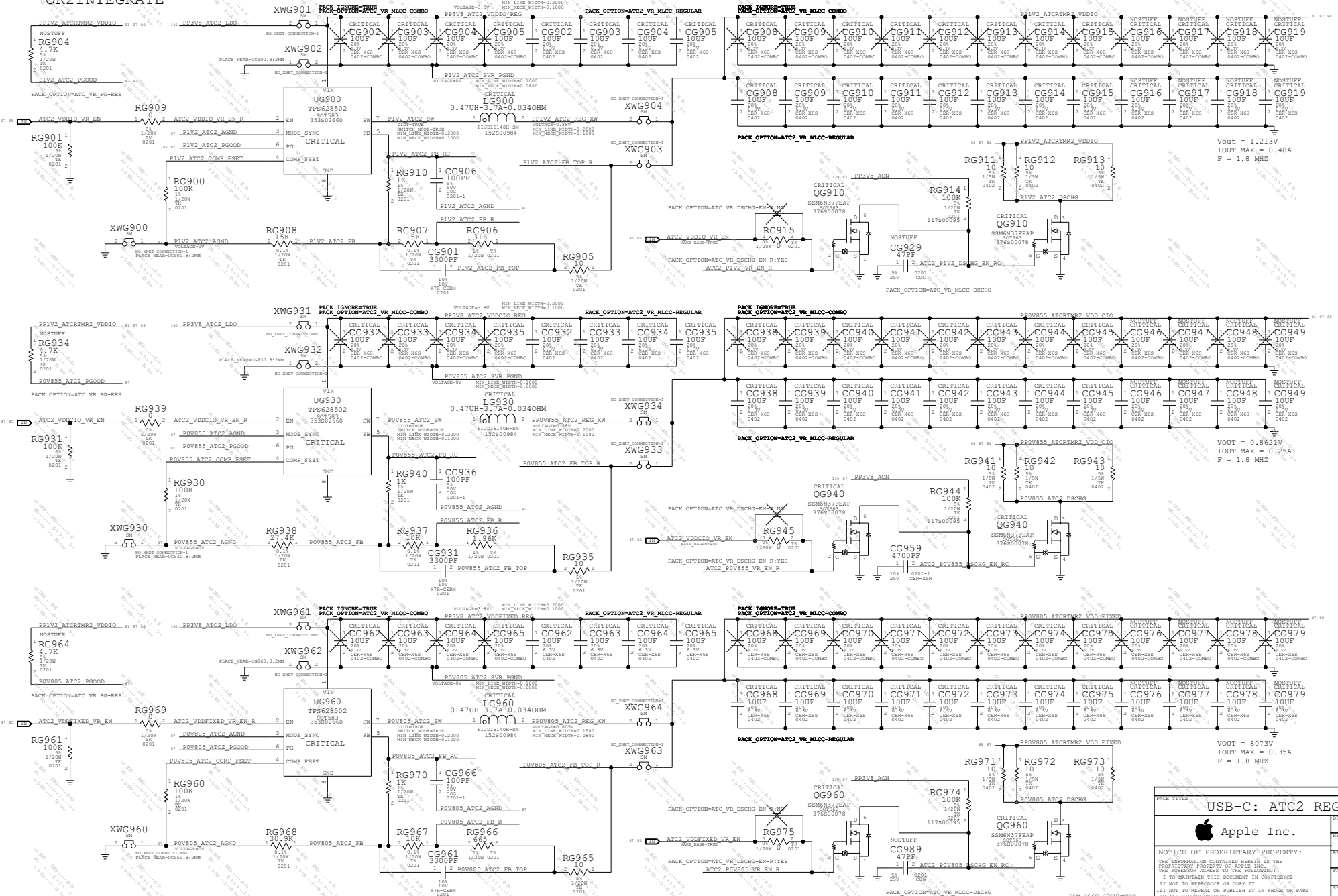
Vout = 5.23V
Freq = 1.9-2.0MHz
OCP Max = 9A
OCP Nom = 7A
OCP Min = 4A
Icc Max = 3.3A



PAGE TITLE: USB-C: 5V Regulator			
 Apple Inc.	051-08012	PAGE	D
	4.0.0	REVISION	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE RECIPIENT AGREES TO THE FOLLOWING: 1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2. NOT TO REPRODUCE OR COPY IT 3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4. ALL RIGHTS RESERVED			
	evt-1	REVISION	
	168 OF 700	PAGE	
	86 OF 159	PAGE	

BOM_COST_GROUP=USB-C

*** OK2INTEGRATE ***

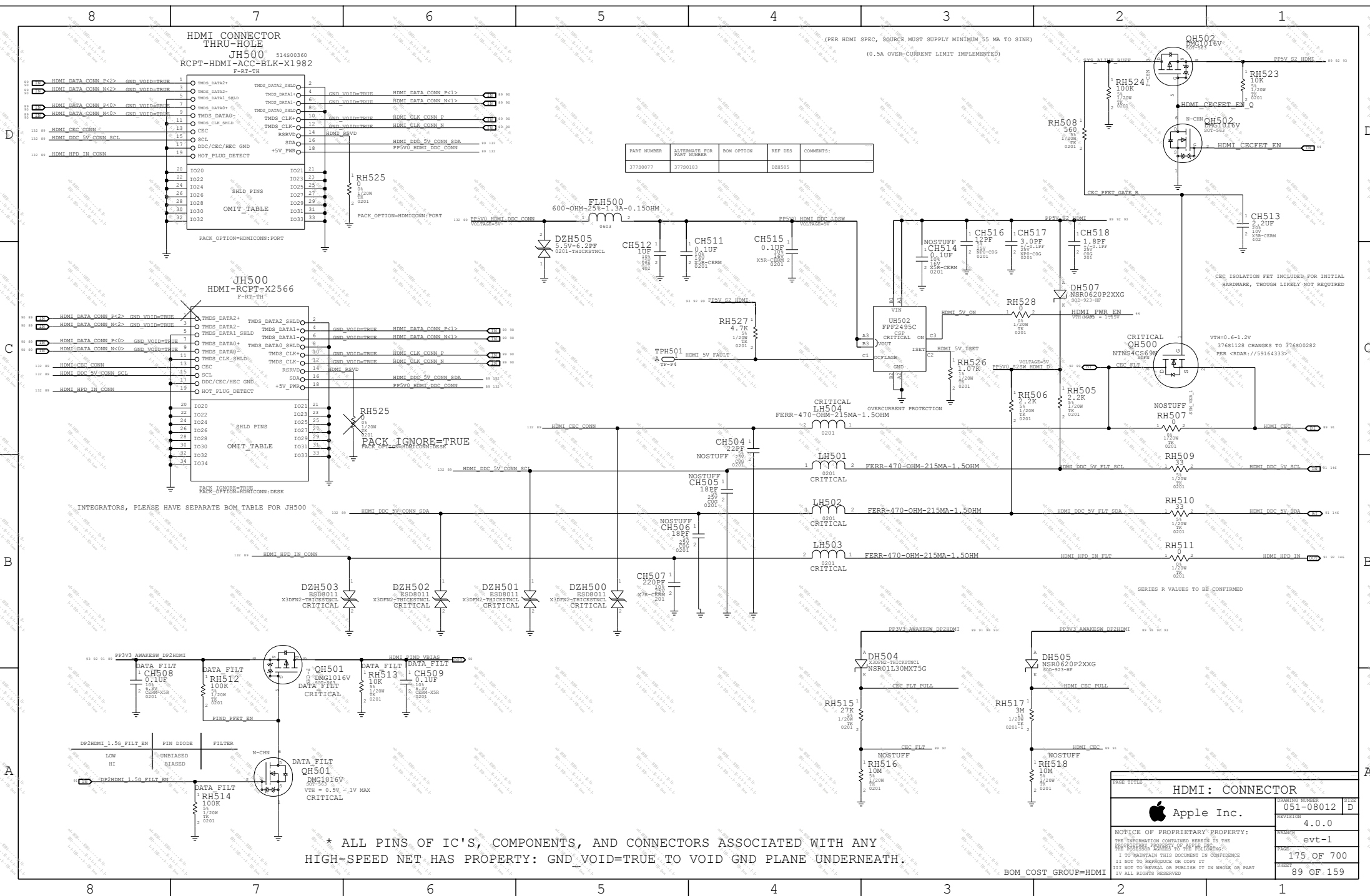


PAGE TITLE			
USB-C: ATC2 REGULATORS			
Apple Inc.	051-08012	REV	D
	4.0.0	REVISION	
NOTICE OF PROPRIETARY PROPERTY:	evt-1	BRANCH	
	169 OF 700	SHEET	
87 OF 159			

VitaminC to LS Alias

FROM REF DESIGN

PAGE TITLE		
USB-C: SUPPORT		
 Apple Inc.	PRODUCT NUMBER	051-08012
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. ONE HORIZON WAY, CUPERTINO, CA 95014 I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I WILL NOT REPRODUCE OR COPY IT I WILL NOT REVEAL OR PUBLISH IT IN WHOLE OR PART I WILL NOT REUSE IT FOR OTHER PURPOSES		DATE evt-1
BOM_COST_GROUP=USB-C		170 OF 700
		88 OF 159



*** OK2INTEGRATE***

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.

D

C

B

A

D

C

B

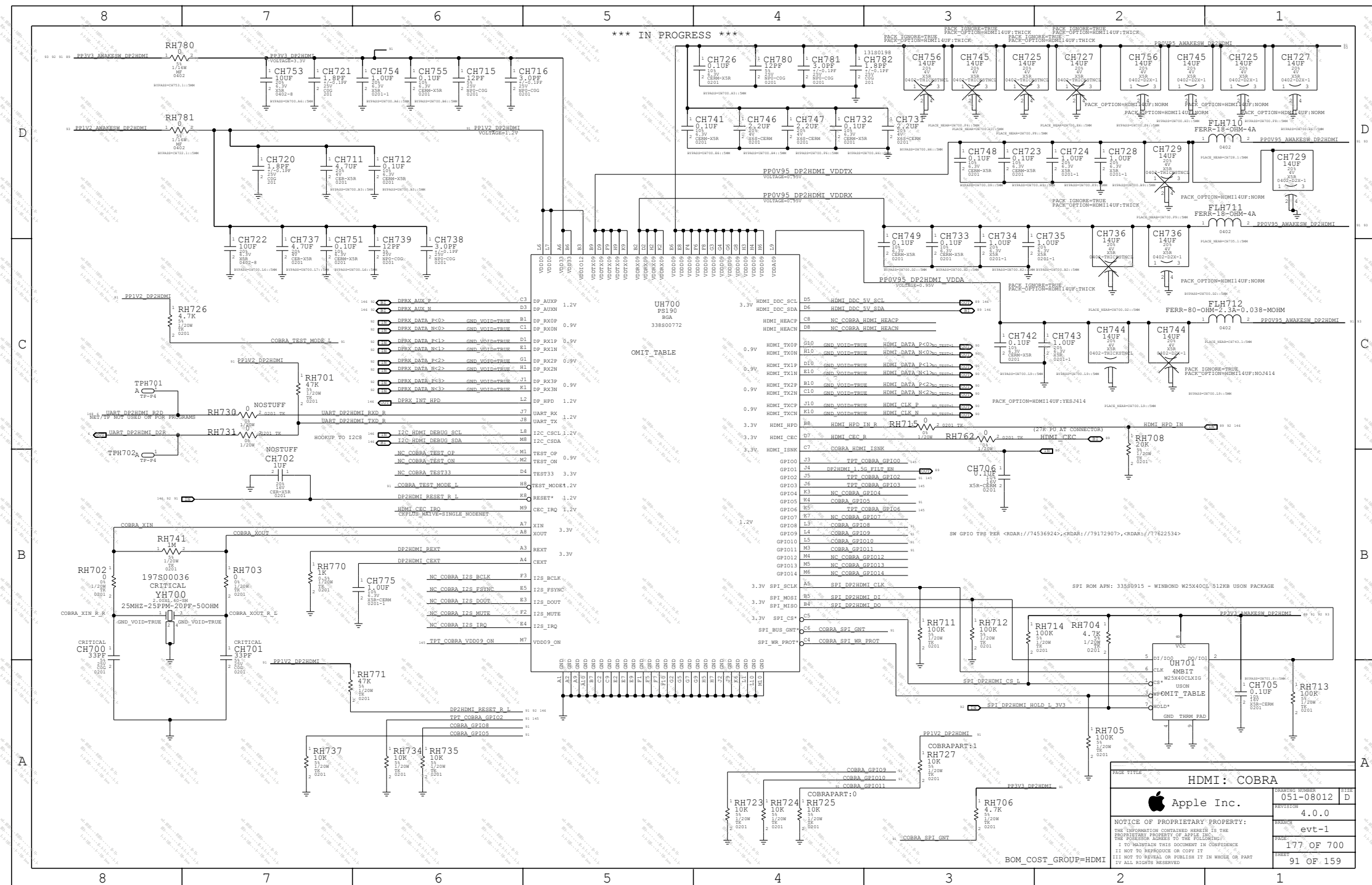
A

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
377800183	4	ESD DIODE, 5.5V, 0.2PF, 0201	DZH600, DZH601, DZH604, DZH607	
377800185	4	ESD DIODE, 5.5V, 0.2PF, 0201	DZH608, DZH611, DZH612, DZH615	
152800850	8	ESD DIODE, 5.5V, 0.2PF, 0201	DZH600, DZH601, DZH604, DZH607	HDMI_CLC_FILT:YES
117800073	8	ESD DIODE, 5.5V, 0.2PF, 0201	DZH600, DZH601, DZH604, DZH607	HDMI_CLC_FILT:NO

FILTER APN NUMBERS
ESD DIODE: 37780178

BOM_COST_GROUP=HDMI

HDMI: DESENSE FILTERS			
Apple Inc.		051-08012	REV D
NOTICE OF PROPRIETARY PROPERTY:		4.0.0	
THE INFORMATION CONTAINED HEREIN IS THE		evt-1	
PROPRIETARY PROPERTY OF APPLE INC.		176 OF 700	
THIS DOCUMENT IS THE PROPERTY OF APPLE INC.		90 OF 159	
IT IS NOT TO BE REPRODUCED OR COPIED			
WITHOUT THE WRITTEN PERMISSION OF APPLE INC.			
IN WHOLE OR IN PART			
ALL RIGHTS RESERVED			

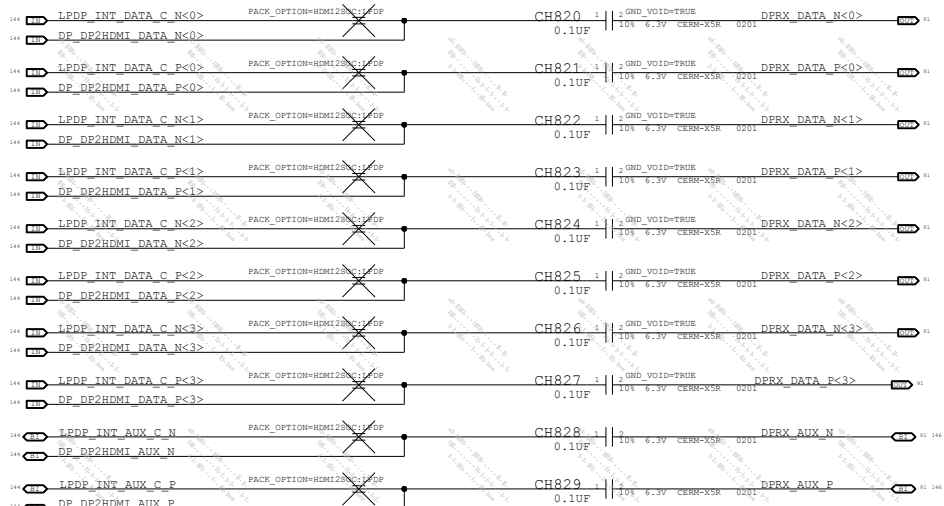


*** IN PROGRESS ***

From SOC

LPDP AC Caps

To HDMI

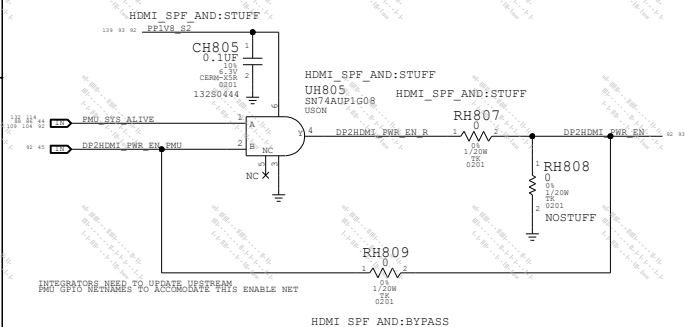


HDMI ROM BOM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
3150913	1	1C, 1M, SPI FLASH ROM, 4MBIT, 1.8V, 0.1uF	UH703	HDMI_ROM12
3150913	1	1C, 1M, SERIAL FLASH, 4MBIT, 1.8V, 0.1uF	UH703	HDMI_ROM1M
34180245	1	ROM, ROM, 1M, (VDD 1.5V, 0.1uF) P1-A/B, 0.1uF	UH701	HDMI_ROM1PREP

THIS IS USED FOR CONTROLLING HDMI PORT POWER VIA THE PMU SYS ALIVE NET

USE THE BYPASS BOMOPTION TO NOT STUFF THESE
OR NO STUFF ALL OF THESE FOR DESKTOPS

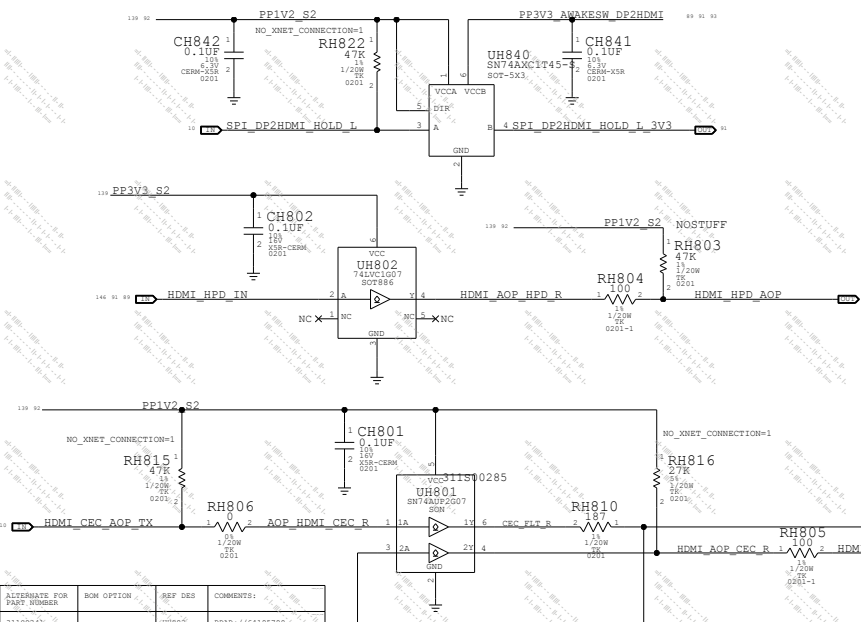


INTEGRATORS NEED TO UPDATE TESTPLAN
PMU GPIO RETURNS TO ACCOMMODATE THIS ENABLE NET

HDMI_SPK_AND:BYPASS

RH908/RH909 intended for potential
resistor divider need after AND gate

LEVEL SHIFTERS

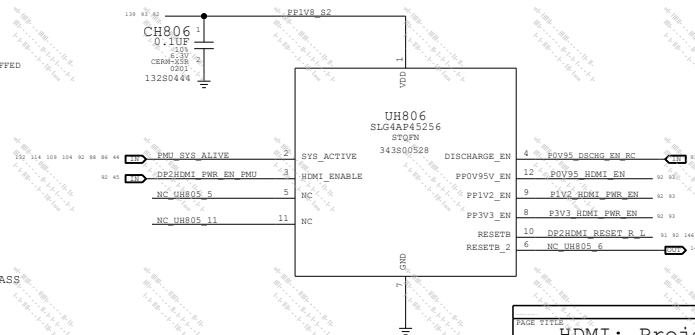
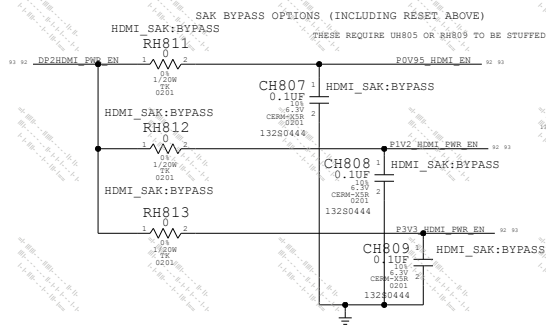


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31180336	31180341		UH802	RDAR://64195790

CONNECT THIS NET TO 5V_S2_MAIN
PLACE THIS HEAD 5V_S2 MAIN VR OUTPUT
NEAR XH801



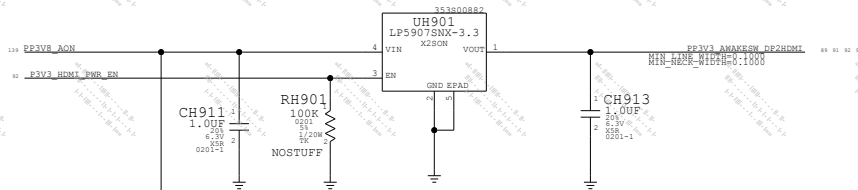
THIS SAK IS USED FOR COBRA POWER SEQUENCING



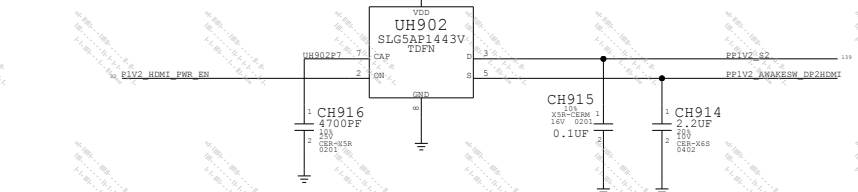
HDMI: Project Support 1			
Apple Inc.		051-08012	D
NOTICE OF PROPRIETARY PROPERTY:		178 OF 700	
THE INFORMATION CONTAINED HEREIN IS THE		92 OF 159	
PROPERTY OF APPLE INC.			
NO REPRODUCTION OR DISSEMINATION			
IS PERMITTED WITHOUT THE EXPRESS			
WRITTEN PERMISSION OF APPLE INC.			
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
2 NOT TO REPRODUCE OR COPY IT			
3 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
4 IN ANY MANNER			
5 IN ANY MANNER			
6 IN ANY MANNER			
7 IN ANY MANNER			
8 IN ANY MANNER			
9 IN ANY MANNER			
10 IN ANY MANNER			
11 IN ANY MANNER			
12 IN ANY MANNER			
13 IN ANY MANNER			
14 IN ANY MANNER			
15 IN ANY MANNER			
16 IN ANY MANNER			
17 IN ANY MANNER			
18 IN ANY MANNER			
19 IN ANY MANNER			
20 IN ANY MANNER			
21 IN ANY MANNER			
22 IN ANY MANNER			
23 IN ANY MANNER			
24 IN ANY MANNER			
25 IN ANY MANNER			
26 IN ANY MANNER			
27 IN ANY MANNER			
28 IN ANY MANNER			
29 IN ANY MANNER			
30 IN ANY MANNER			
31 IN ANY MANNER			
32 IN ANY MANNER			
33 IN ANY MANNER			
34 IN ANY MANNER			
35 IN ANY MANNER			
36 IN ANY MANNER			
37 IN ANY MANNER			
38 IN ANY MANNER			
39 IN ANY MANNER			
40 IN ANY MANNER			
41 IN ANY MANNER			
42 IN ANY MANNER			
43 IN ANY MANNER			
44 IN ANY MANNER			
45 IN ANY MANNER			
46 IN ANY MANNER			
47 IN ANY MANNER			
48 IN ANY MANNER			
49 IN ANY MANNER			
50 IN ANY MANNER			
51 IN ANY MANNER			
52 IN ANY MANNER			
53 IN ANY MANNER			
54 IN ANY MANNER			
55 IN ANY MANNER			
56 IN ANY MANNER			
57 IN ANY MANNER			
58 IN ANY MANNER			
59 IN ANY MANNER			
60 IN ANY MANNER			
61 IN ANY MANNER			
62 IN ANY MANNER			
63 IN ANY MANNER			
64 IN ANY MANNER			
65 IN ANY MANNER			
66 IN ANY MANNER			
67 IN ANY MANNER			
68 IN ANY MANNER			
69 IN ANY MANNER			
70 IN ANY MANNER			
71 IN ANY MANNER			
72 IN ANY MANNER			
73 IN ANY MANNER			
74 IN ANY MANNER			
75 IN ANY MANNER			
76 IN ANY MANNER			
77 IN ANY MANNER			
78 IN ANY MANNER			
79 IN ANY MANNER			
80 IN ANY MANNER			
81 IN ANY MANNER			
82 IN ANY MANNER			
83 IN ANY MANNER			
84 IN ANY MANNER			
85 IN ANY MANNER			
86 IN ANY MANNER			
87 IN ANY MANNER			
88 IN ANY MANNER			
89 IN ANY MANNER			
90 IN ANY MANNER			
91 IN ANY MANNER			
92 IN ANY MANNER			
93 IN ANY MANNER			
94 IN ANY MANNER			
95 IN ANY MANNER			
96 IN ANY MANNER			
97 IN ANY MANNER			
98 IN ANY MANNER			
99 IN ANY MANNER			
100 IN ANY MANNER			

BOM_COST_GROUP=HDMI

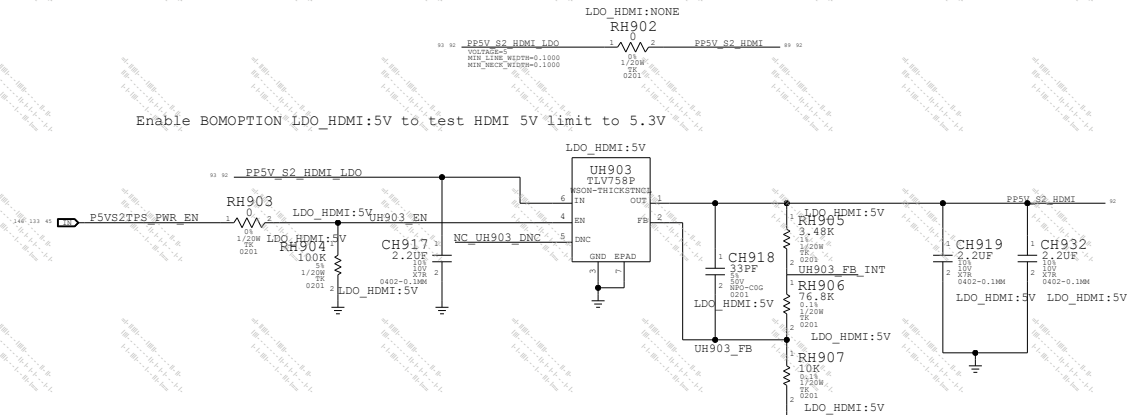
3.3V LDO



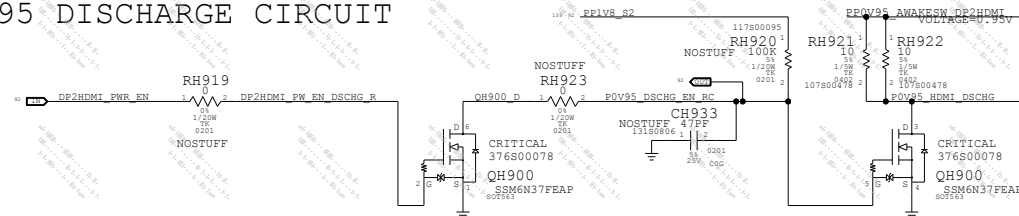
1.2V LOAD SW



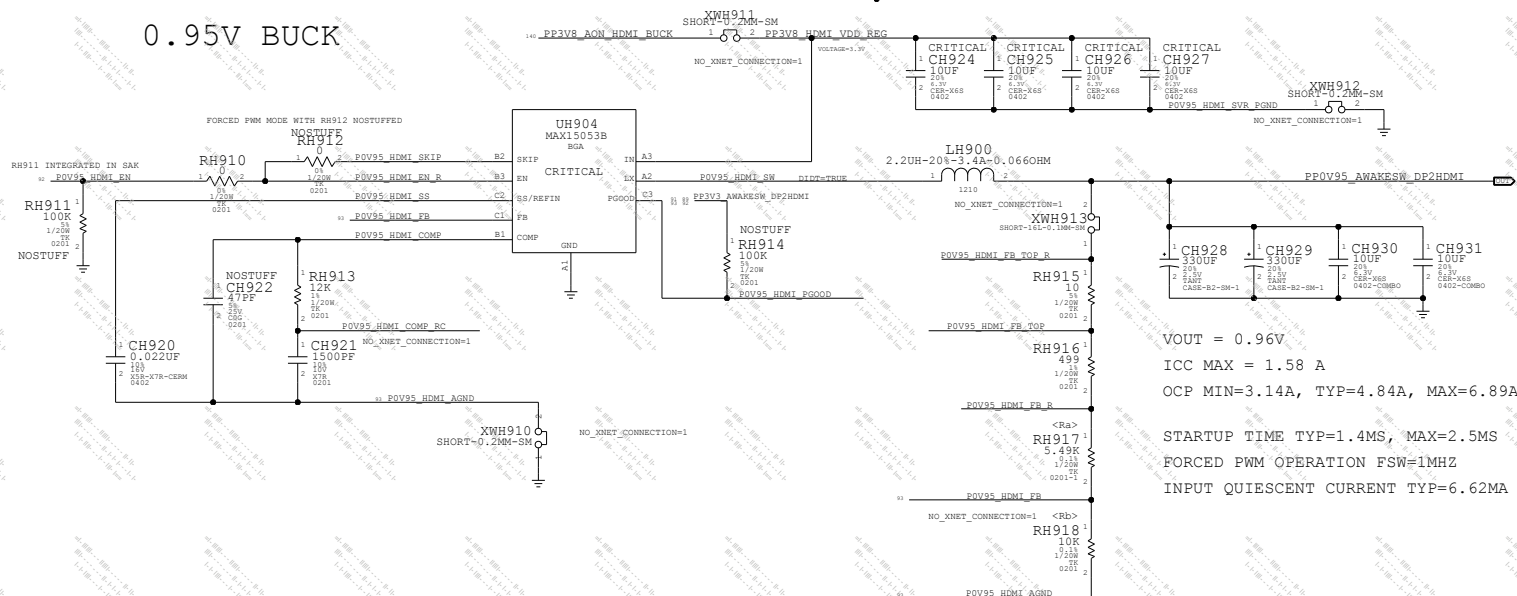
THIS IS USED FOR LONGER 5V POWER PATHS TO ENSURE GOOD 5V REGULATION
Enable BOMOPTION LDO_HDMI:NONE to disable the LDO use



0.95 DISCHARGE CIRCUIT

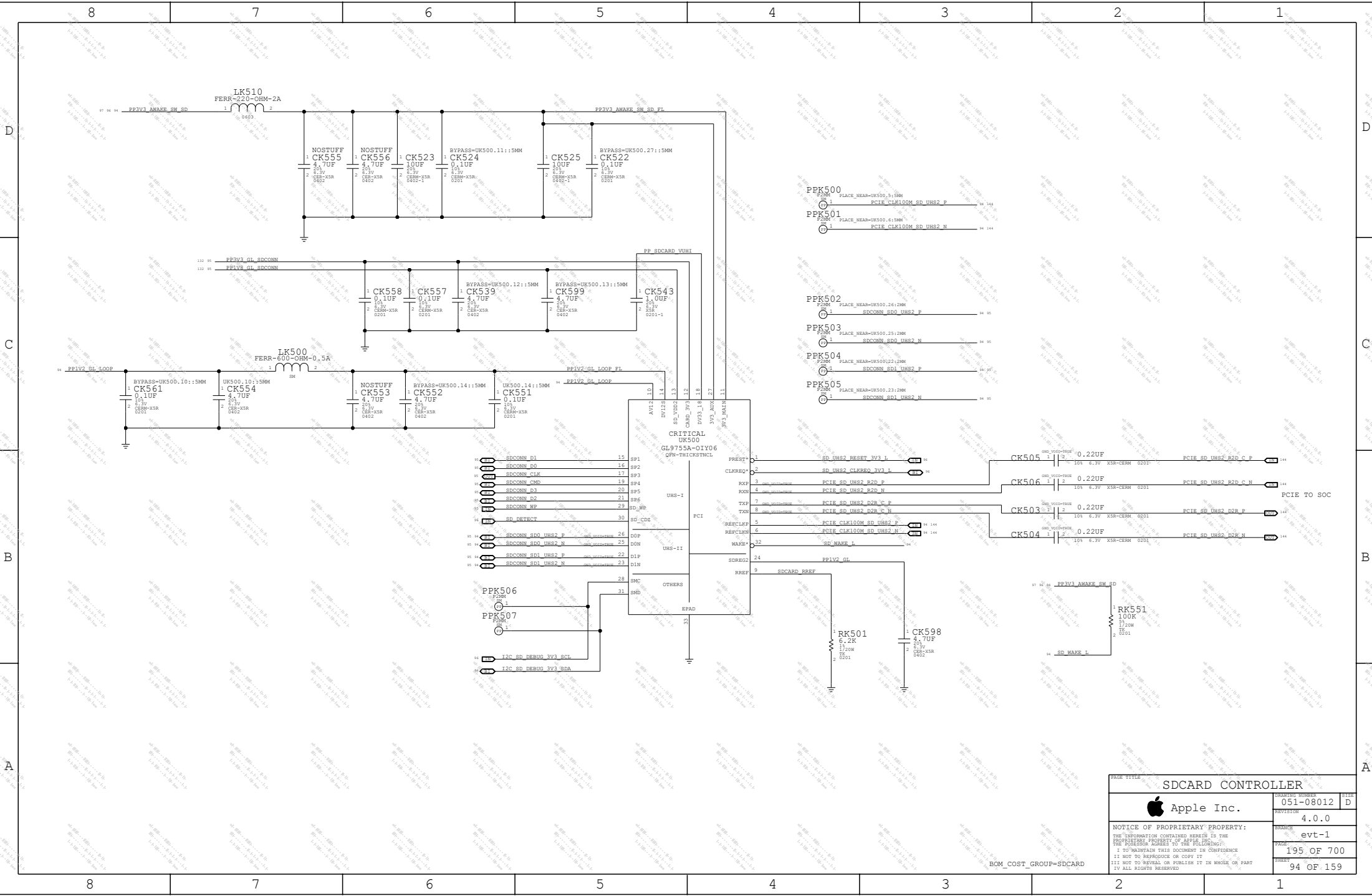


0.95V BUCK



VOUT = 0.96V
ICC MAX = 1.58 A
OCP MIN=3.14A, TYP=4.84A, MAX=6.89A
STARTUP TIME TYP=1.4MS, MAX=2.5MS
FORCED PWM OPERATION FSW=1MHZ
INPUT QUIESCENT CURRENT TYP=6.62MA

PAGE TITLE			
HDMI: Project Support 2			
Apple Inc.	051-08012	REV	D
	4.0.0	REVISION	
	evt-1	STAGE	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE RECIPIENT AGREES TO THE FOLLOWING:			
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
2. NOT TO REPRODUCE OR COPY IT			
3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
4. ALL RIGHTS RESERVED			
179 OF 700			
93 OF 159			



PAGE TITLE		
SDCARD CONTROLLER		
 Apple Inc.	REVISION NUMBER	051-08012
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. ONE HORIZON AVENUE, CUPERTINO, CA 95014 © 2011 APPLE INC. ALL RIGHTS RESERVED.	REVISION	evt-1
	PAGE	195 OF 700
	PAGE	94 OF 159

BOM_COST_GROUP=SDCARD

SD CARD CONNECTOR 514-00196

CONN. FOR J314 USED AS REF. ONLY
CHECK CONN. FOR YOUR SPECIFIC PROJECT
PLEASE HAVE SEPARATE BOM TABLE FOR JK600

INTEGRATORS,

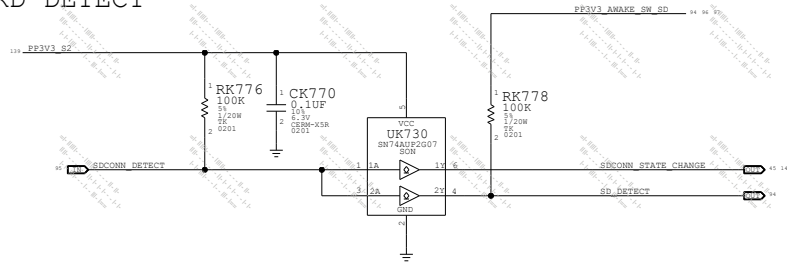
OMIT TABLE
JK600
RCPT-BLK-SHIFT-SD-X1982
F-RT-TR

SD MODE	PCIE MODE
1 CD/DAT3	PERST*
2 CMD	NU
3 VSS1	VSS1
4 VDD	VDD1
5 CLK*	NU
6 VSS2	VSS2
7 DAT0	REFCLK+
8 DAT1	REFCLK-
9 DAT2	CLKREQ*
10 NU	VSS3
11 NU	PCIE TX+
12 NU	PCIE TX-
13 NU	VSS4
14 NU	VDD2
15 NU	PCIE RX-
16 NU	PCIE RX+
17 NU	VSS5
18 NU	VDD3
19 NC*	WP SWITCH
20 INS DET SW	INS DET SW
21	
22 SHIELD	
23 SHIELD	
24 SHIELD	
25 SHIELD	
26 SHIELD	
27 SHIELD	
28 SHIELD	
29 SHIELD	
30 SHIELD	
31 SHIELD	

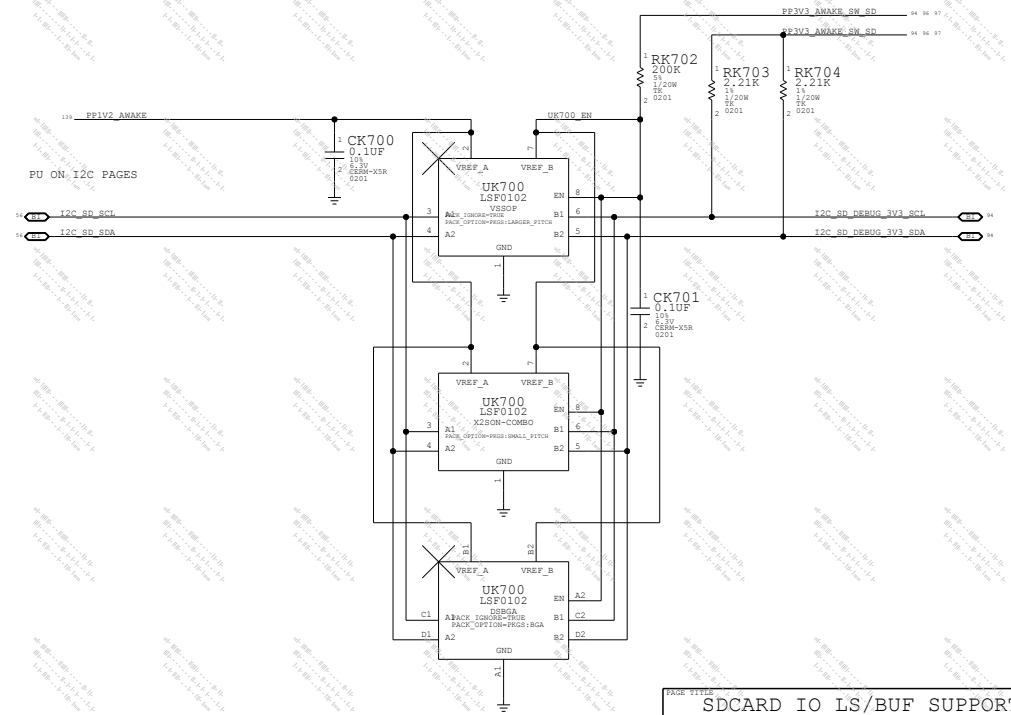
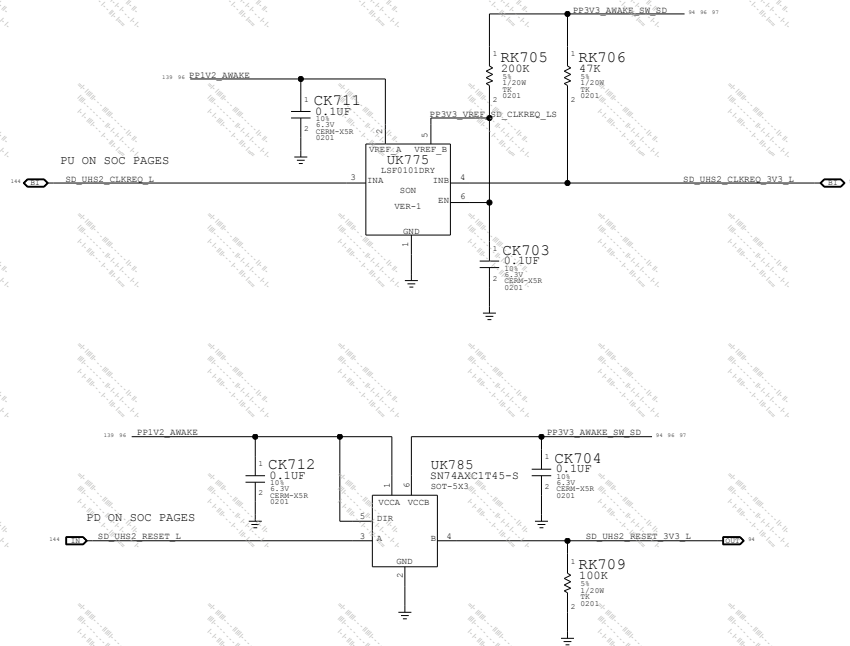
SDCARD CONNECTOR		
 Apple Inc.	051-08012	051-08012
	4.0.0	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.	evt-1	196 OF 700
	95 OF 159	

BOM_COST_GROUP=SDCARD

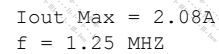
CARD DETECT



CONTROLLER IO



PAGE TITLE			
SDCARD IO LS/BUF SUPPORT			
	REVISION NUMBER		051-08012
	REVISION		4.0.0
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS TO REMAIN IN CONFIDENCE. THE FOLLOWS ARE THE TERMS OF THE CONFIDENTIALITY AGREEMENT:			
1. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
2. NOT TO REPRODUCE OR COPY IT			
3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
4. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
5. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
6. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
7. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
8. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
9. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
10. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
11. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
12. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
13. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
14. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
15. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
16. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
17. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
18. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
19. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
20. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
21. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
22. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
23. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
24. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
25. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
26. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
27. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
28. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
29. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
30. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
31. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
32. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
33. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
34. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
35. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
36. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
37. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
38. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
39. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
40. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
41. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
42. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
43. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
44. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
45. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
46. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
47. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
48. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
49. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
50. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
51. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
52. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
53. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
54. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
55. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
56. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
57. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
58. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
59. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
60. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
61. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
62. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
63. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
64. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
65. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
66. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
67. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
68. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
69. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
70. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
71. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
72. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
73. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
74. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
75. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
76. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
77. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
78. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
79. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
80. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
81. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
82. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
83. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
84. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
85. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
86. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
87. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
88. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
89. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
90. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
91. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
92. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
93. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
94. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
95. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
96. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
97. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
98. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
99. TO MAINTAIN THE INFORMATION IN CONFIDENCE			
100. TO MAINTAIN THE INFORMATION IN CONFIDENCE			

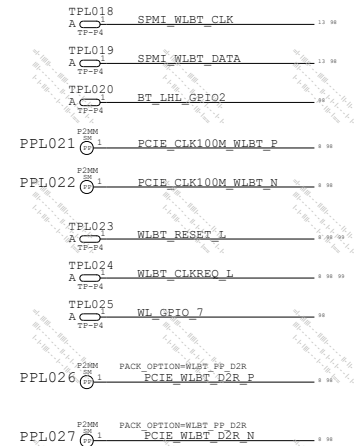
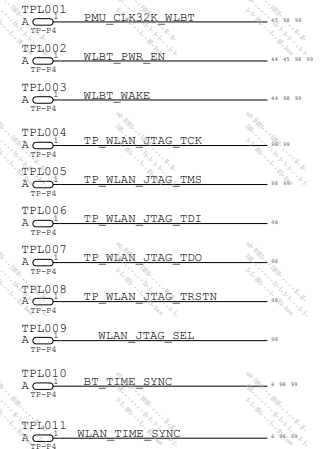
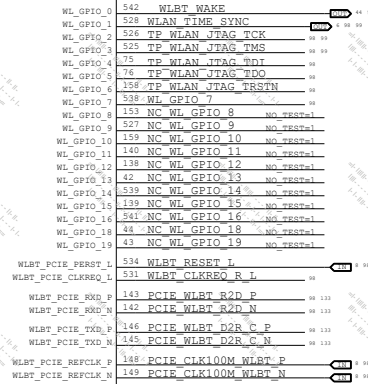
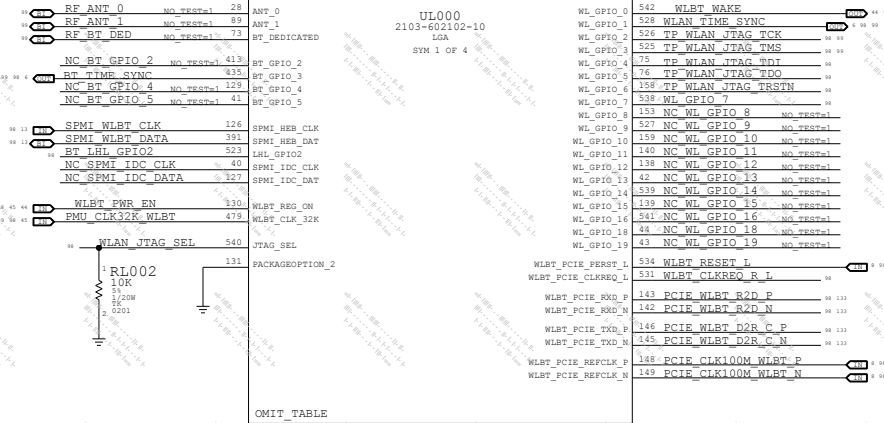
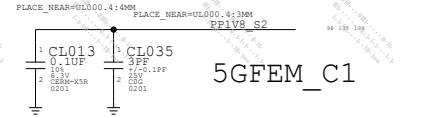
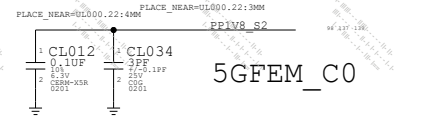
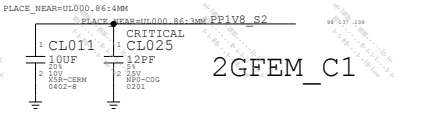
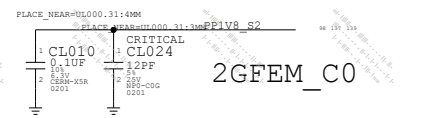
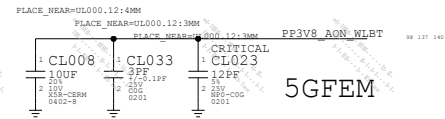
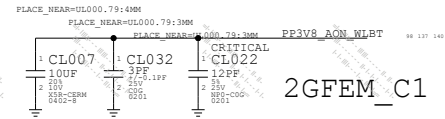
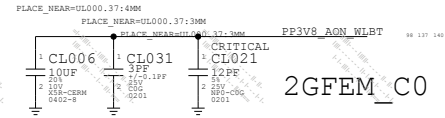
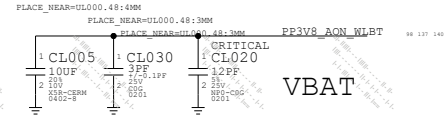


BOM_COST_GROUP=SDCARD

*** OK2INTEGRATE ***

FOR SYSTEM INTEGRATION INFORMATION OF WILLAMETTE REFER TO
RDAR://PROBLEM/72432057

WILLAMETTE WIFI/BT MODULE



WILLAMETTE BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33901093	1	MODULE, WLAN/BT, WILLAMETTE, 604.7	UL000	CRITICAL	



BOM_COST_GROUP=WIRESLESS

PAGE TITLE		
WIFI/BT: MODULE		
	ORIGIN: NUMBER	051-08012
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY:		
THE INFORMATION CONTAINED HEREIN IS THE		
PROPERTY OF APPLE INC. AND IS NOT TO BE		
REPRODUCED OR COPIED IN ANY MANNER		
WITHOUT THE WRITTEN PERMISSION OF APPLE INC.		
THIS DOCUMENT IS UNCLASSIFIED		
DATE 11/11/2011 BY 111111		
ALL RIGHTS RESERVED		
PAGE		200 OF 700
PAGE		98 OF 159

*** OK2INTEGRATE ***

WILLAMETTE WIFI/BT MODULE GND

ANTENNA CONNECTORS

2G_C0
5G_C0
BT_C0

2G_C1
5G_C1
BT_C1

BT_C1_DED

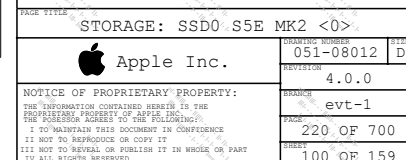
WLBT DEBUG CONNECTOR

RF CONNECTOR ALTERNATE BOM:

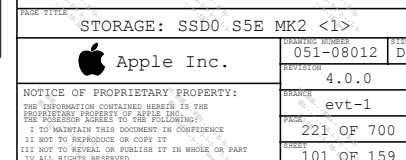
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
5180067	51800033	RFCONN_ALT	ALL	IPEX

WIFI/BT: ANTENNA and GND		REVISION	051-08012	D
Apple Inc.		REVISION	4.0.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE REVISIONS LISTED AT THE BOTTOM OF THIS PAGE 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE DO NOT TO REPRODUCE OR COPY IT DO NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IN ANY MANNER		REVISION	evt-1	
		PAGE	201 OF 700	
		PAGE	99 OF 159	

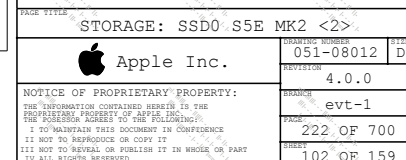
NAND0 S5E0



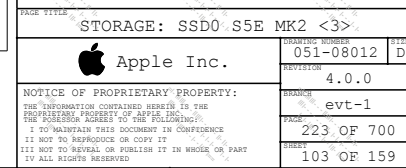
NAND0 S5E1



NAND0 S5E2

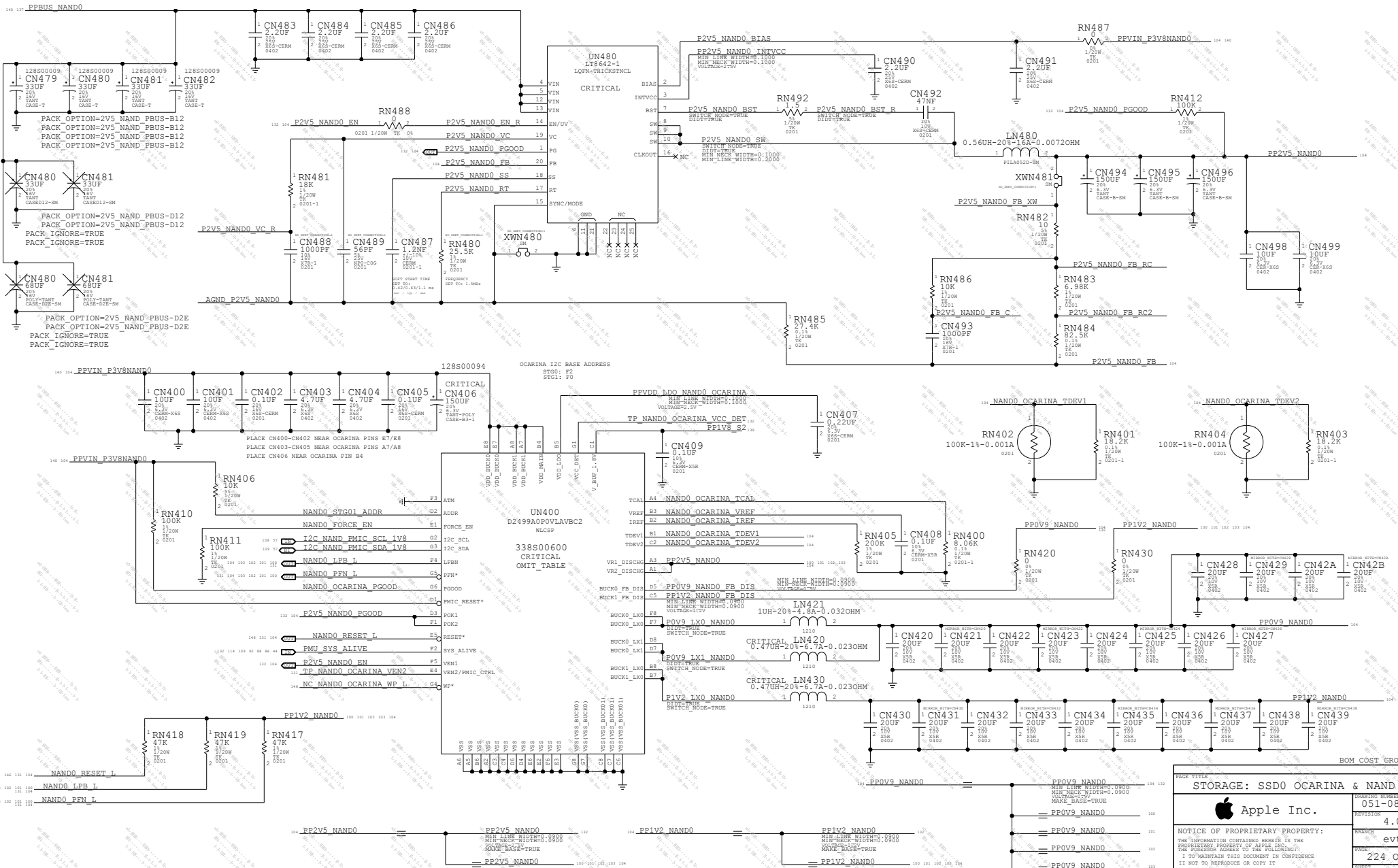


NAND0 S5E3



BOM_COST_GROUP=SSD

*** OK2 INTEGRATE ***

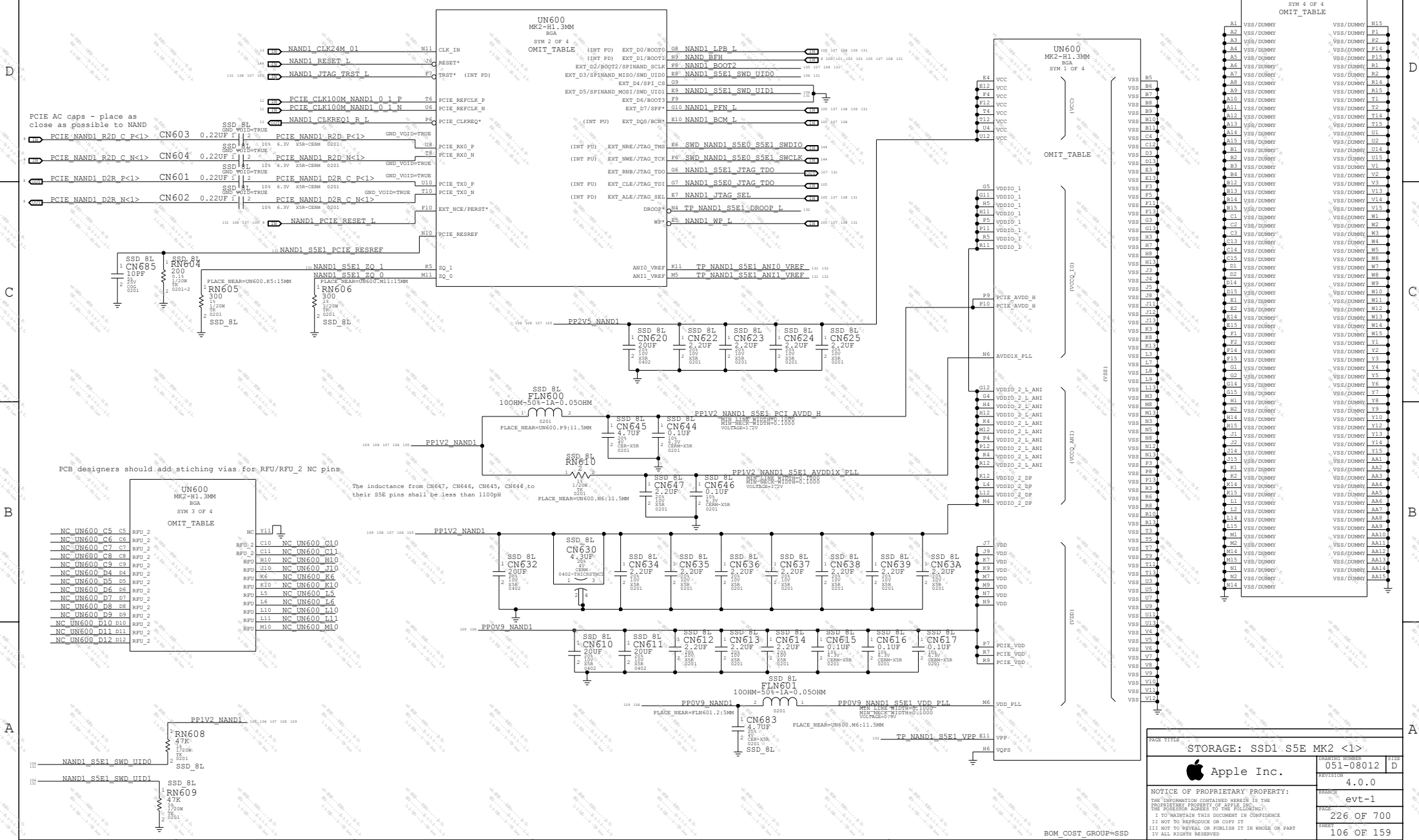


NAND1	S5E0
-------	------



*** OK2INTEGRATE ***

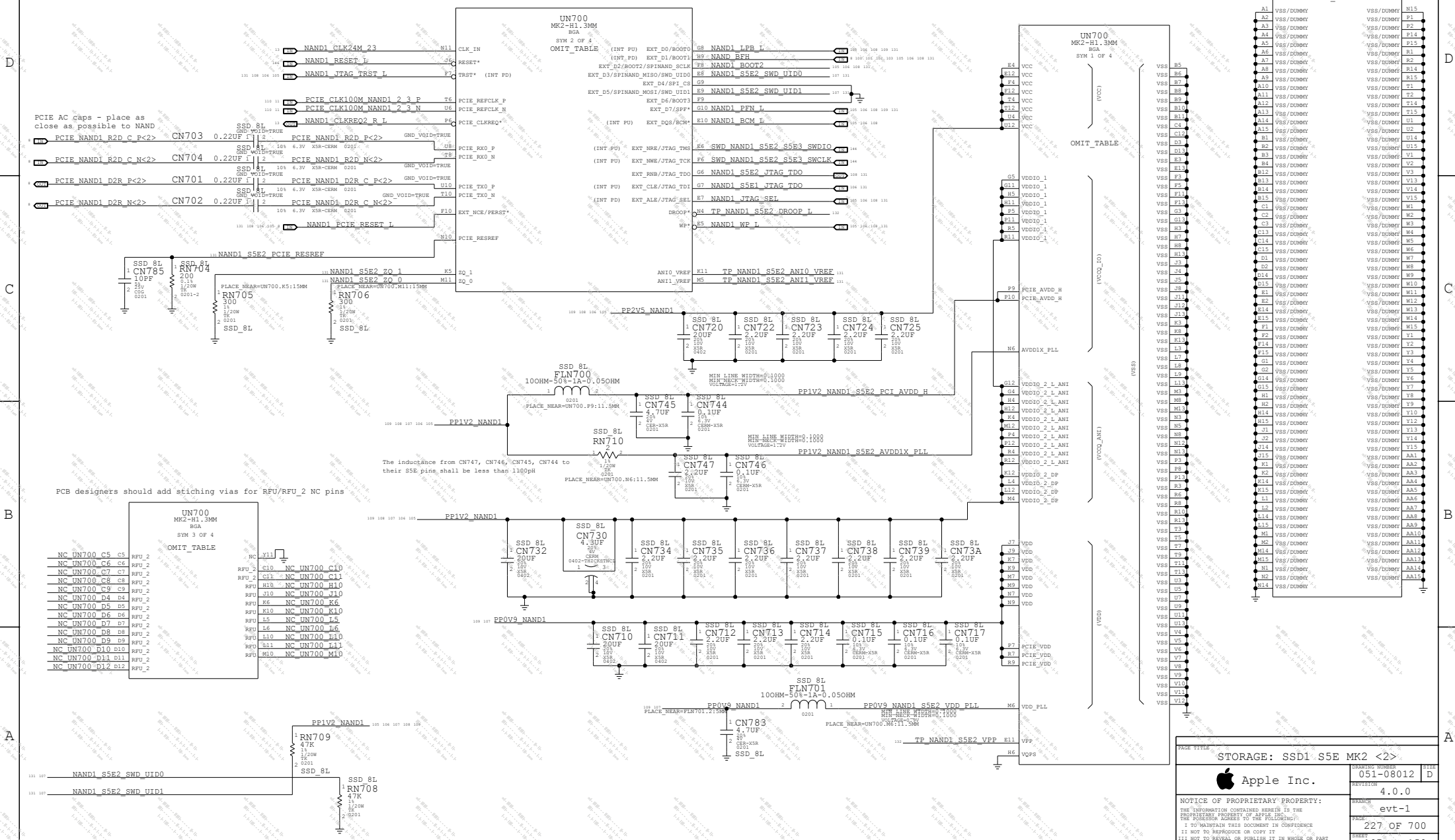
NAND1 S5E1



PAGE TITLE	
STORAGE: SSD1 S5E MK2 <1>	
Apple Inc.	051-08012
	4.0.0
Apple Inc.	evt-1
	226 OF 700
Apple Inc.	106 OF 159

*** OK2INTEGRATE ***

NAND1 S5E2

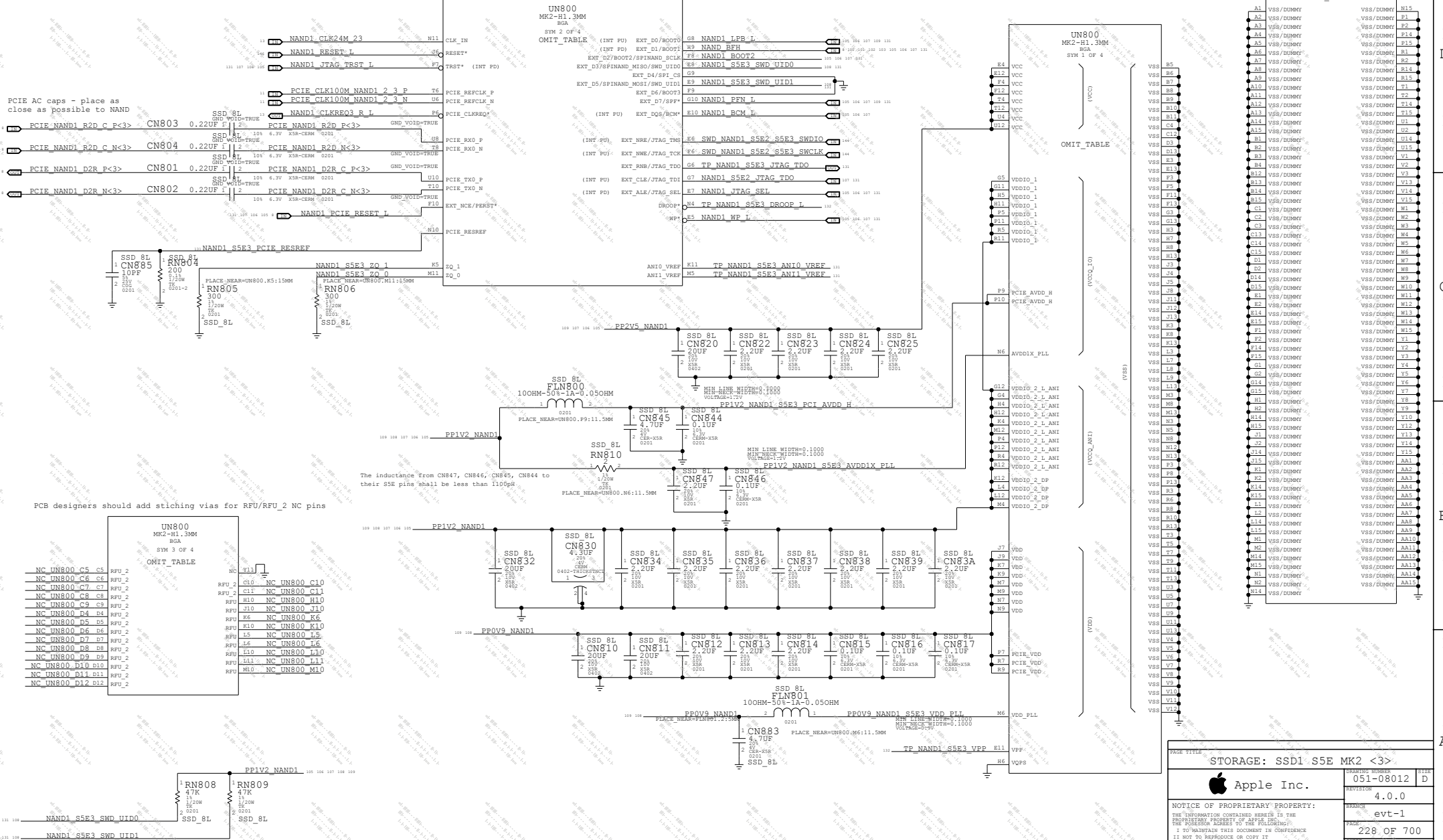


PAGE TITLE		STORAGE: SSD1 S5E MK2 <2>	
Apple Inc.		051-08012	REV D
NOTICE OF PROPRIETARY PROPERTY:		4.0.0	
THE INFORMATION CONTAINED HEREIN IS THE		evt-1	
PROPRIETARY PROPERTY OF APPLE INC.		227 OF 700	
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		107 OF 159	
11 NOT TO REPRODUCE OR COPY IT			
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
112 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
113 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
114 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
115 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
116 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
117 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
118 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
119 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
120 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			

BOM_COST_GROUP=SSD

*** OK2INTEGRATE ***

NAND1 S5E3



BOM_COST_GROUP=SSD

PAGE TITLE		STORAGE: SSD1 S5E MK2 <3>	
Apple Inc.		051-08012	
NOTICE OF PROPRIETARY PROPERTY:		4.0.0	
11 NOT TO REPRODUCE OR COPY IT		evt-1	
11 NOT TO REPRODUCE OR COPY IT		228 OF 700	
11 NOT TO REPRODUCE OR COPY IT		108 OF 159	

D



PAGE TITLE:		STORAGE: SSD1 OCARINA & NAND VCC	
	Apple Inc.		DRAWING NUMBER 051-08012
			REVISION 4.0.0
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE FOLLOWING AGREEMENT TO BE FULFILLED:			
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2. NOT TO REPRODUCE OR COPY IT 3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4. ALL RIGHTS RESERVED			
		DRAWING NAME 229 OF 700	REV 109 OF 159

D

C

B

A

D

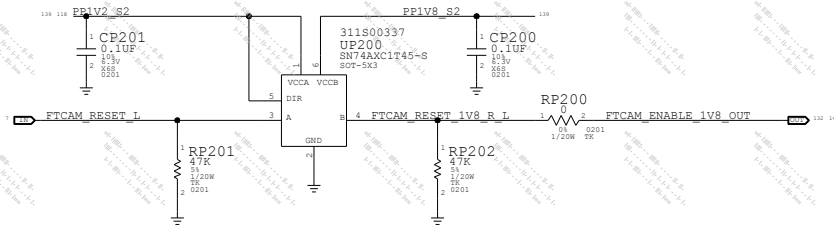
C

B

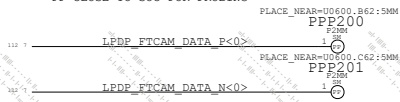
LA

BOM_COST_GROUP=SSD

Level Shifter - FTCAM

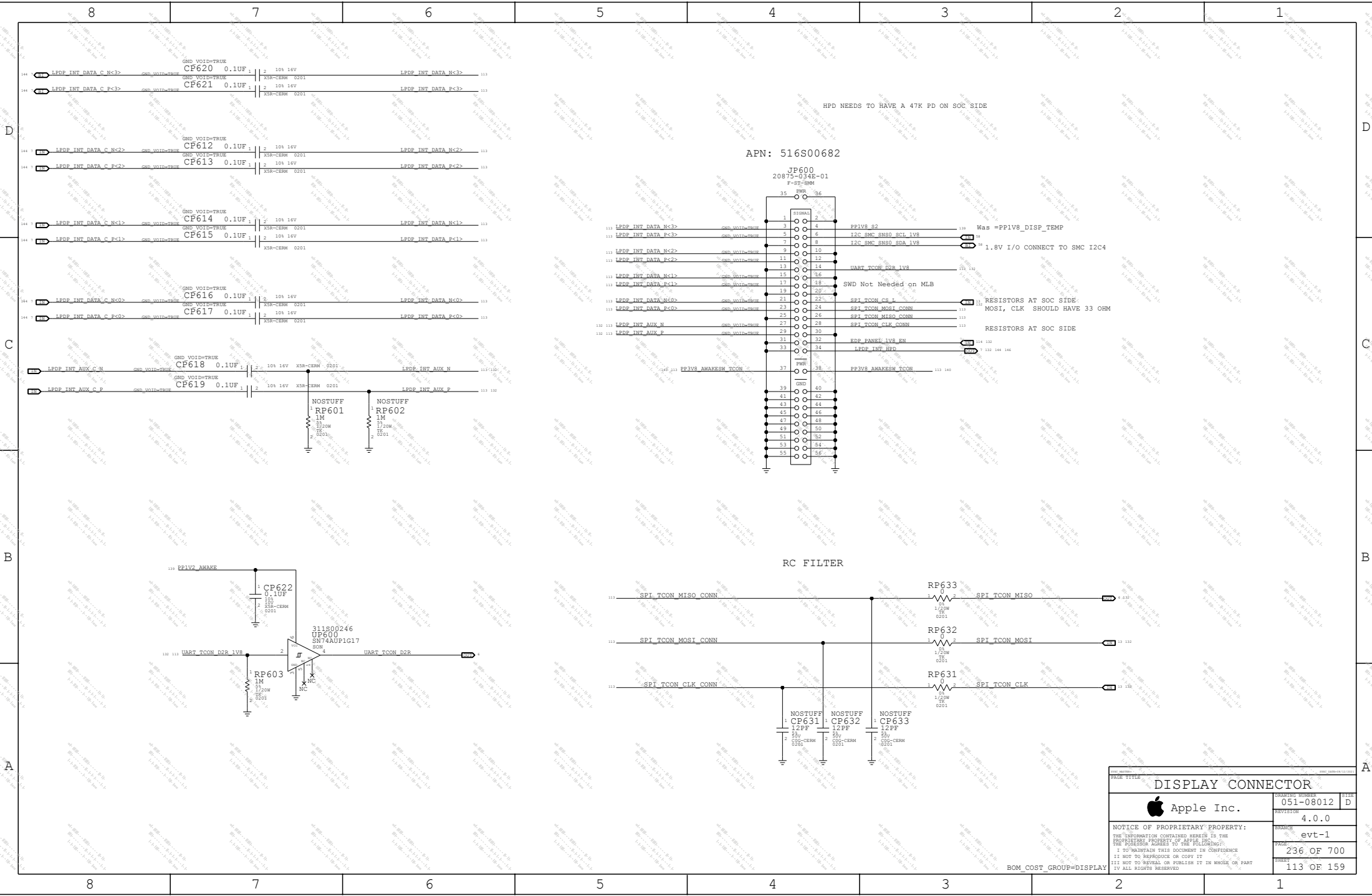


PP CLOSE TO SOC FOR PROBING



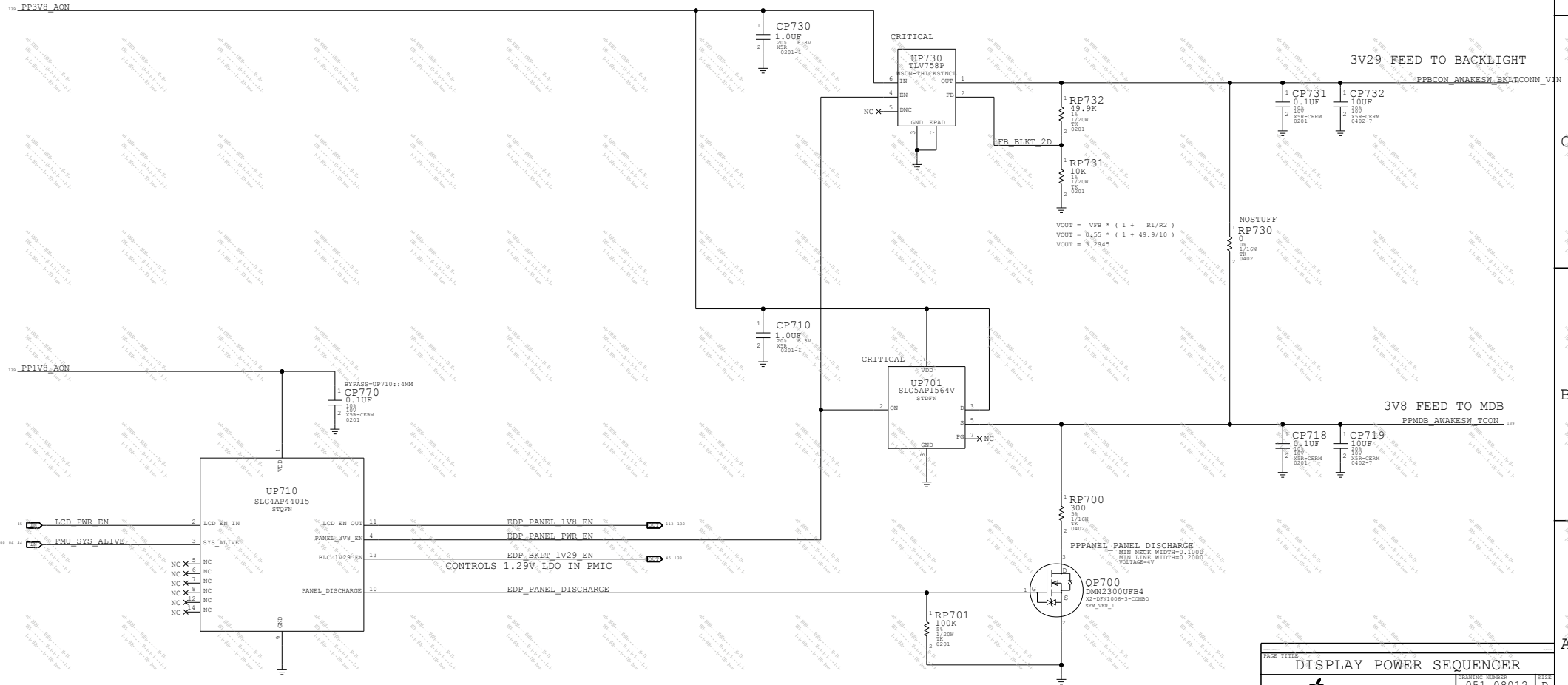
BOM_COST_GROUP=CAMERA

CAMERA-SUPPORT			
Apple Inc.		051-08012	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.		4.0.0	evt-1
232 OF 700		111 OF 159	



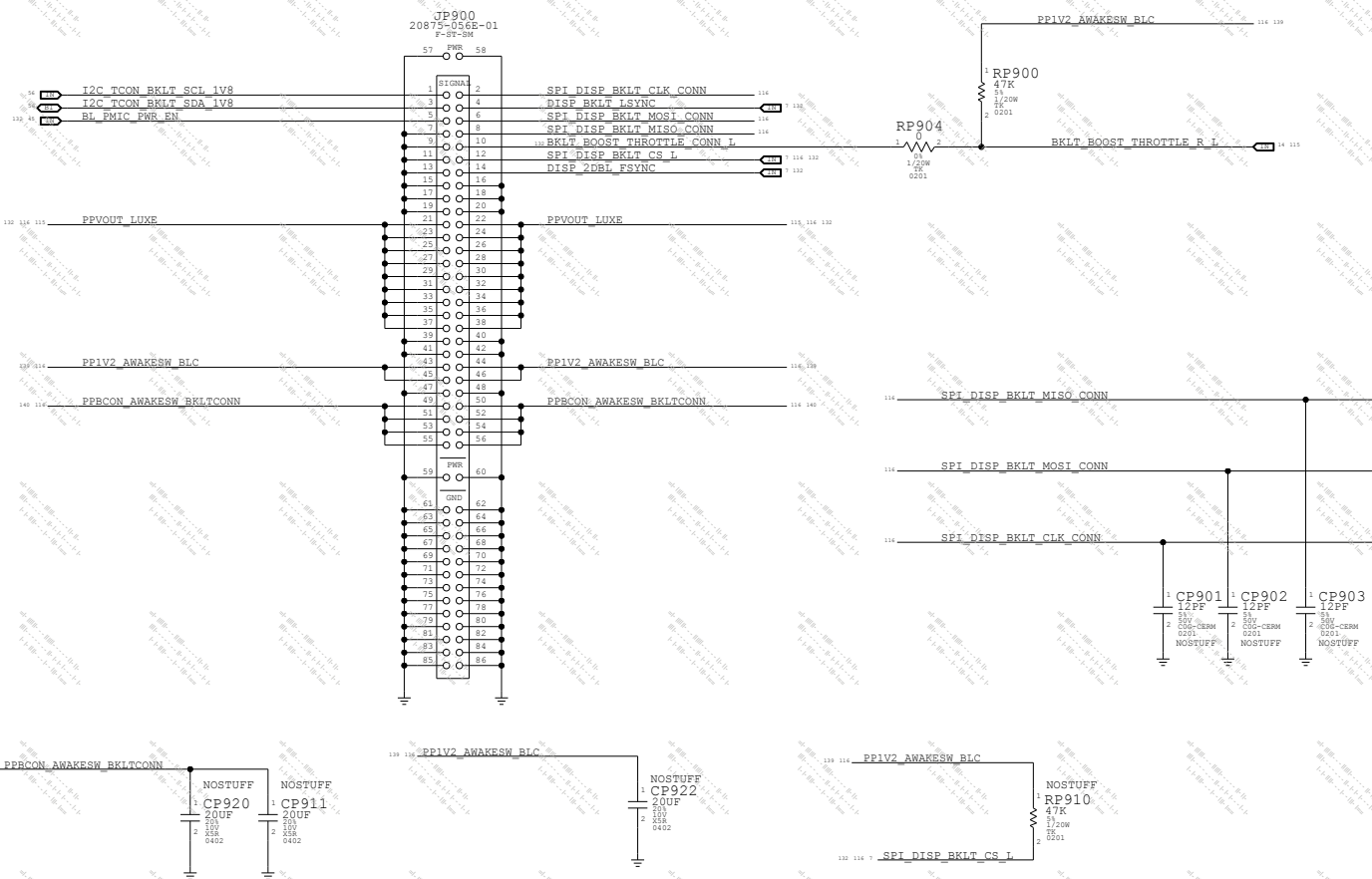
PAGE TITLE		PAGE NUMBER (1 OF 159)	
DISPLAY CONNECTOR			
 Apple Inc.	CREATING NUMBER	051-08012	TYPE
	REVISION		D
		4.0.0	
NOTICE OF PROPRIETARY PROPERTY:		TRAINING	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE RECIPIENT AGREES TO THE FOLLOWING:		evt-1	
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		PAGE	
2. NOT TO REPRODUCE OR COPY IT		236 OF 700	
3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		SECRET	
4. ALL RIGHTS RESERVED		113 OF 159	

*** OK2INTEGRATE ***



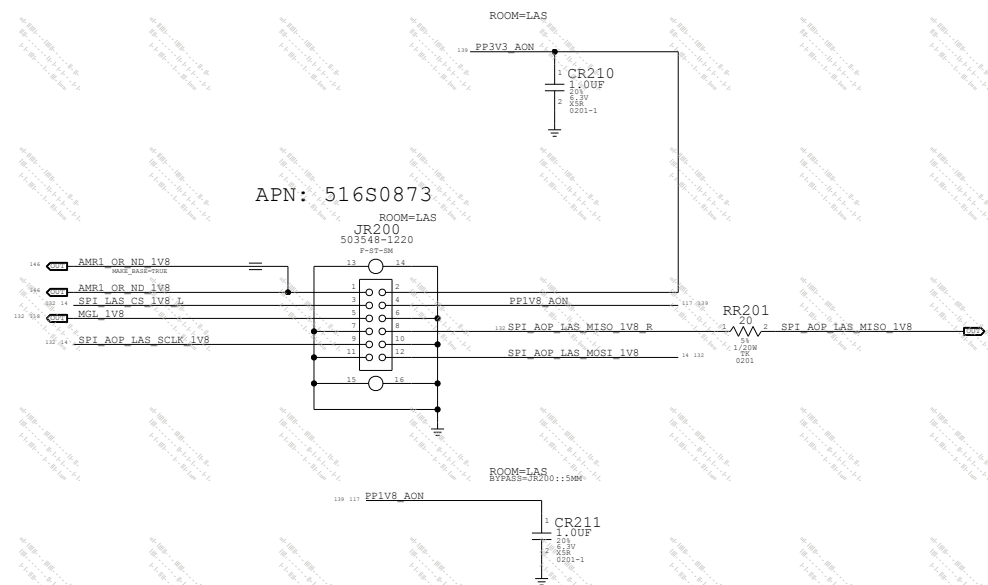
DISPLAY POWER SEQUENCER			
Apple Inc.	051-08012	PAGE D	
	4.0.0		
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE RECIPIENT AGREES TO THE FOLLOWING: 1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2. NOT TO REPRODUCE OR COPY IT 3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4. ALL RIGHTS RESERVED	evt-1	237 OF 700	
		114 OF 159	

BOM_COST_GROUP=DISPLAY



BCON CONNECTOR			
Apple Inc.		051-08012	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. ALL RIGHTS ARE RESERVED. NO PART OF THIS DOCUMENT SHALL BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION SYSTEMS.		4.0.0	
239 OF 700		evt-1	
116 OF 159			

*** OK2INTEGRATE ***



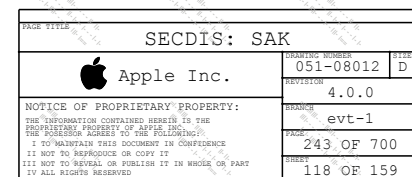
CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	22UA	1.2MA
1.8 AON	30UA	8 MA
3.3 AON	1UA	10 MA

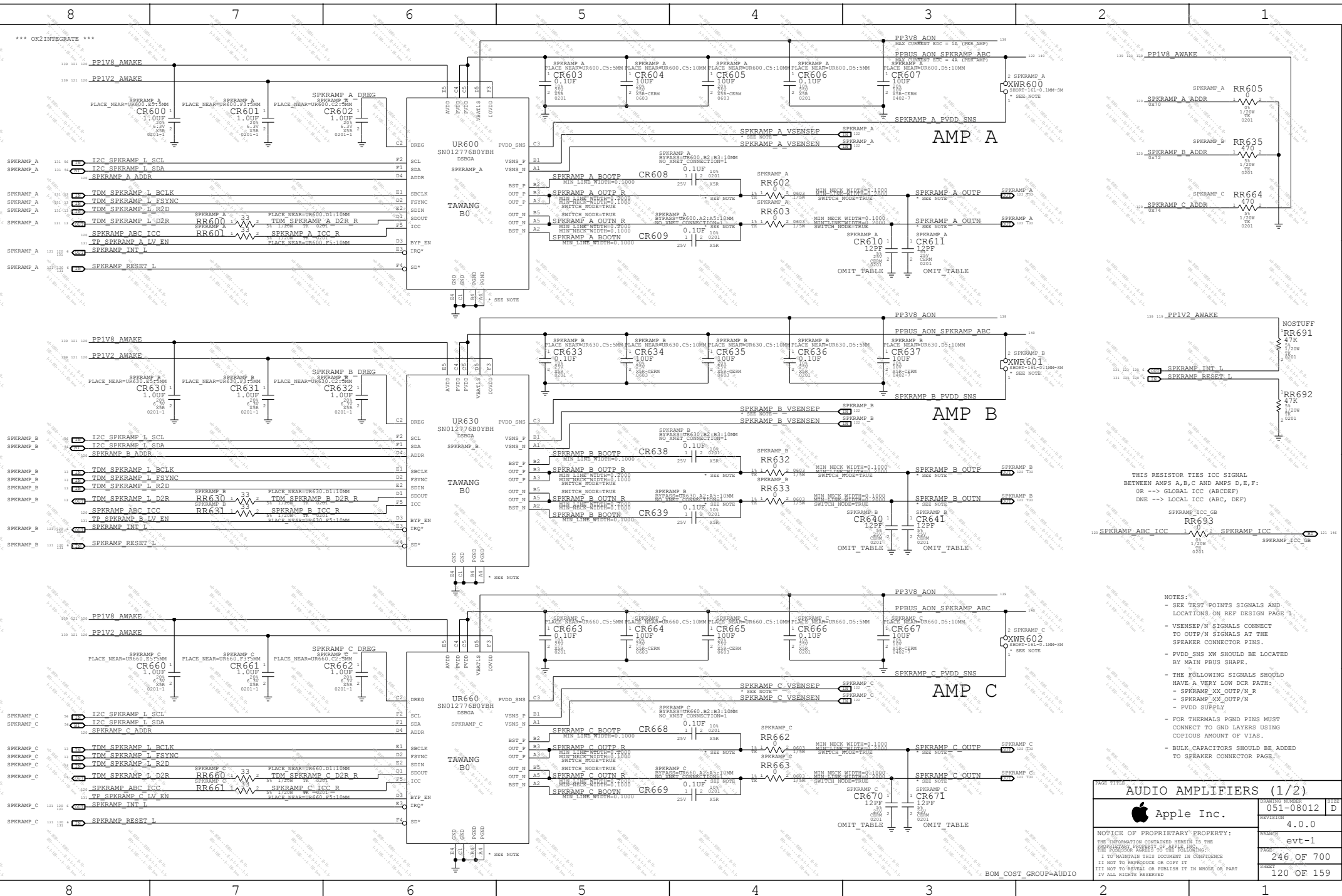
PAGE TITLE		SECDIS: LID ANGLE SENSOR	
REVISION		051-08012	D
NOTICE OF PROPRIETARY PROPERTY:		Apple Inc.	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE REVISIONS AGREE TO THE FOLLOWING:		4.0.0	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		evt-1	
I NOT TO REPRODUCE OR COPY IT		242 OF 700	
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		117 OF 159	
I ALL RIGHTS RESERVED			

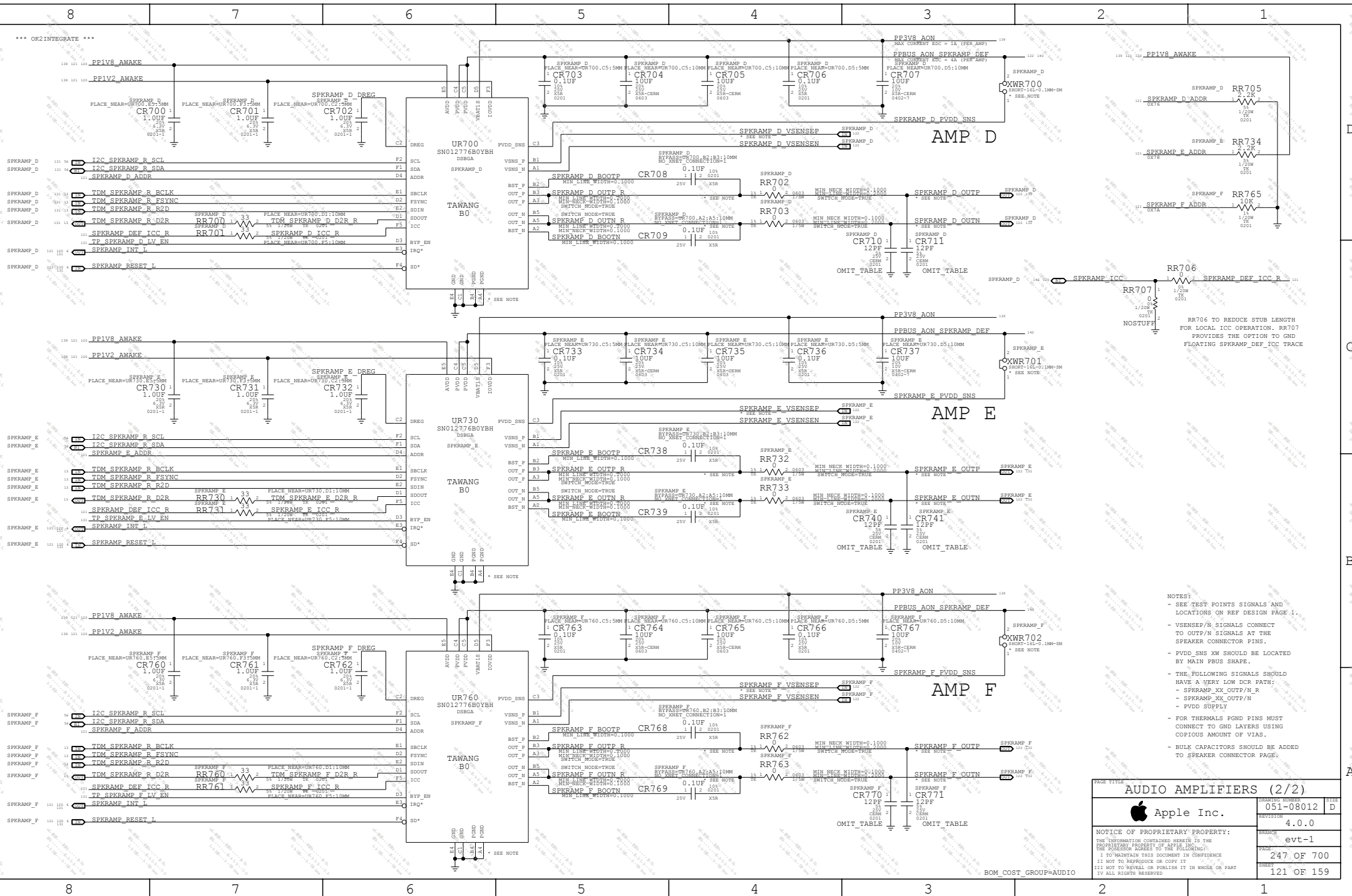
BOM_COST_GROUP=SOC

LID SECDIS LOGIC

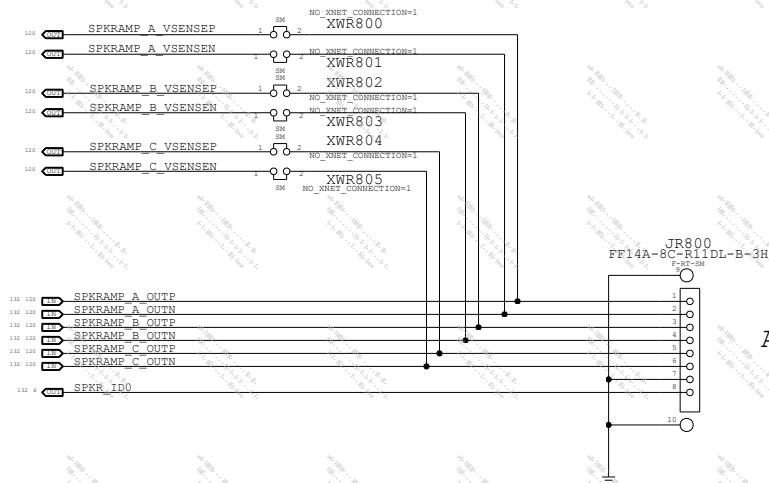


BOM COST GROUP=SOC





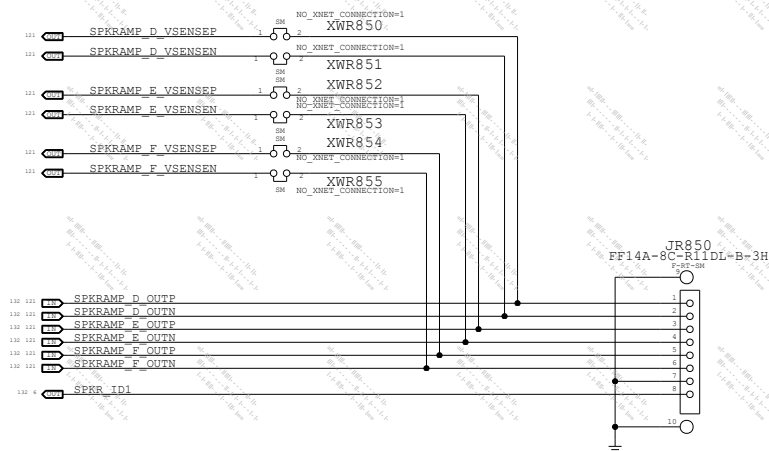
LEFT AUDIO SPEAKER CONNECTOR



L Woofer 1
L Woofer 2
L Tweeter

APN: 518S00164

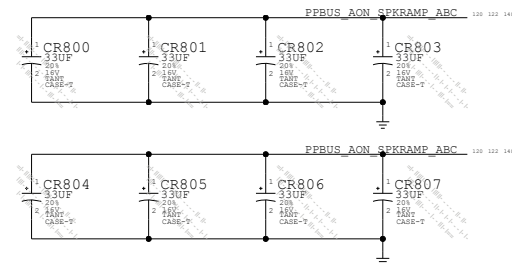
RIGHT AUDIO SPEAKER CONNECTOR



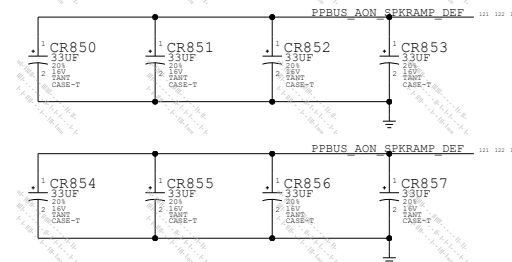
R Woofer 1
R Woofer 2
R Tweeter

APN: 518S00164

LEFT AMPLIFIERS BULK CAPACITANCE



RIGHT AMPLIFIERS BULK CAPACITANCE

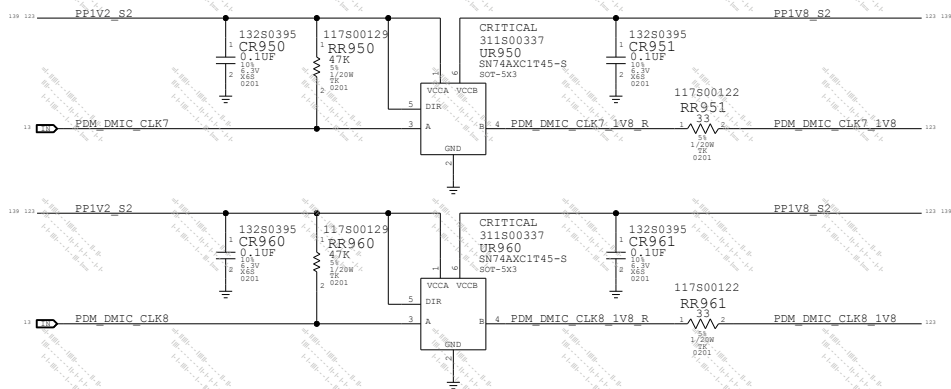


PAGE TITLE			
AUDIO CONNECTORS: AMPS			
Apple Inc.	051-08012	DATE	D
	4.0.0	REVISION	
NOTICE OF PROPRIETARY PROPERTY:		ISSUANCE	evt-1
THE INFORMATION CONTAINED HEREIN IS THE		FIGURE	248 OF 700
PROPERTY OF APPLE INC.		FIGURE	122 OF 159
THE INFORMATION CONTAINED HEREIN IS THE			
PROPERTY OF APPLE INC.			
THE INFORMATION CONTAINED HEREIN IS THE			
PROPERTY OF APPLE INC.			
THE INFORMATION CONTAINED HEREIN IS THE			
PROPERTY OF APPLE INC.			

BOM_COST_GROUP=AUDIO

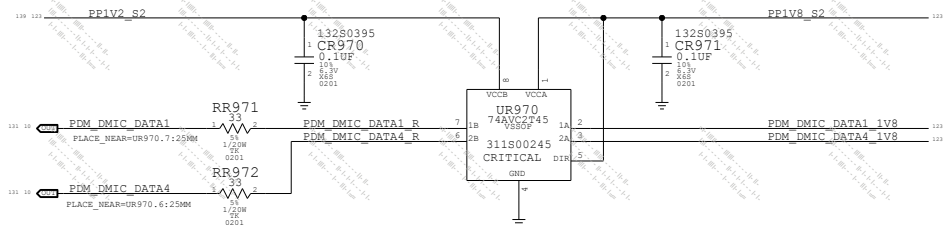
LEVEL SHIFTERS: DMIC CLOCK

TWO SEPARATE SINGLE BIT LS FOR XTALK CONCERNS <RDAR://70058941> -- MAY CHANGE TO DUAL SHIFTER



LEVEL SHIFTER: DMIC DATA

HIGH ON DIR IS A -> B
BOTH A AND B SIDE CAN BE ANY VOLTAGE FROM 0.8 TO 3.6

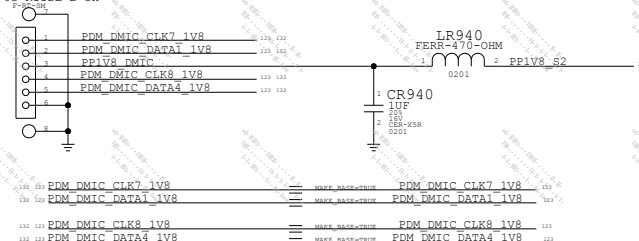


Digital Mic Flex Connector

APN: 51850818

JR940

FF14A-6C-R11DL-B-3H



Audio Jack Flex Connector

PART_NUMBER=516S1181

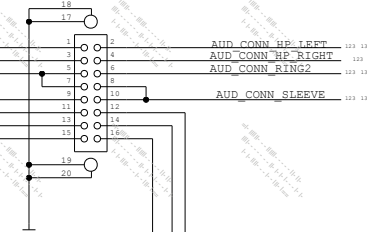
JR900

AA250-S015V1

P-27-2M

APN: 516S1181, MATING PLUG APN: 516S1180

SAME AS J314

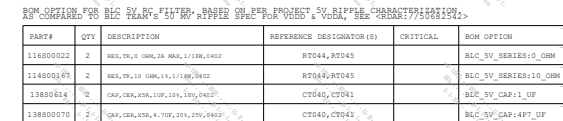


LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE: AUDIO FLEX CONNECTORS		
Apple Inc.	051-08012	PAGE D
	4.0.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE EXPRESS WRITTEN PERMISSION OF APPLE INC.	evt-1	
	249 OF 700	
123 OF 159		

BOM_COST_GROUP=AUDIO

BEN IC: KEYBOARD LED DRIVER



UT001.4: V_{OH} MIN = 2.3V
V_{OL} MAX = 0.1V @ P_{WM} KEYS I MAX OF 10A

PP3V3_S2
PP1V2_S2

PLACE_HEADER=UT001.4;R000;PLACE_HEADER=UT001.4;R000

CT000 1
0.1UF
160
X5R-63V
0201

CT001 1
0.1UF
160
X5R-63V
0201

311S00337
UT001
SN74AXC1T45-S
SOP-3X3

UT000.12 V_{IR} MIN 1.7V
V_{IR} MAX 1.4V

RT001
0
1/20W
5%
0201

KBD_BKLT_PWM
KBD_BKLT_PWM_R

RT000
47K
1/20W
5%
0201

UT001.3:
V_{IR} MIN = V_{CCA} X 0.65 = 0.78V

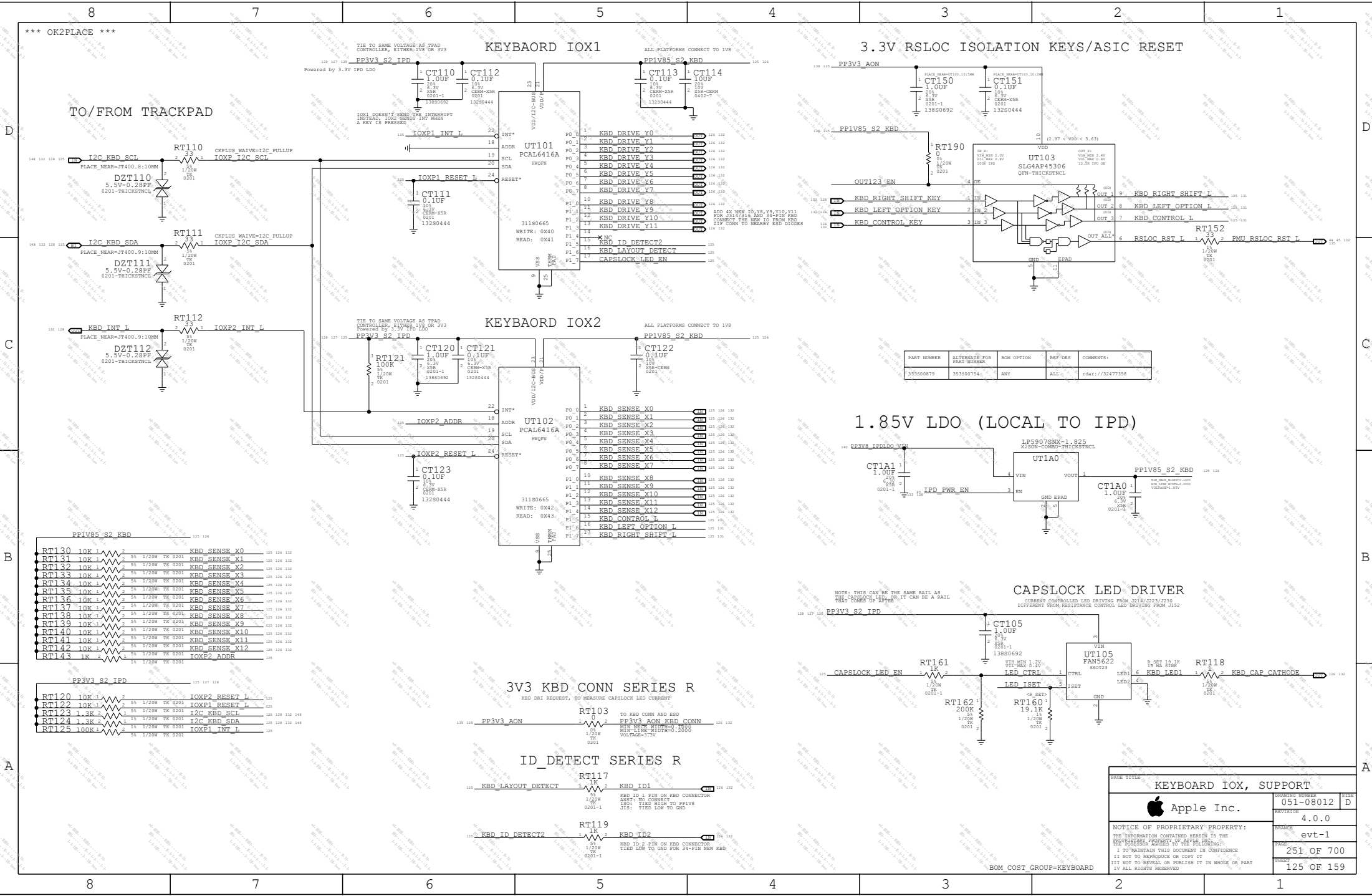
KBD_BKLT_PWM_3V3

GND

GND KBD BKLT SGND

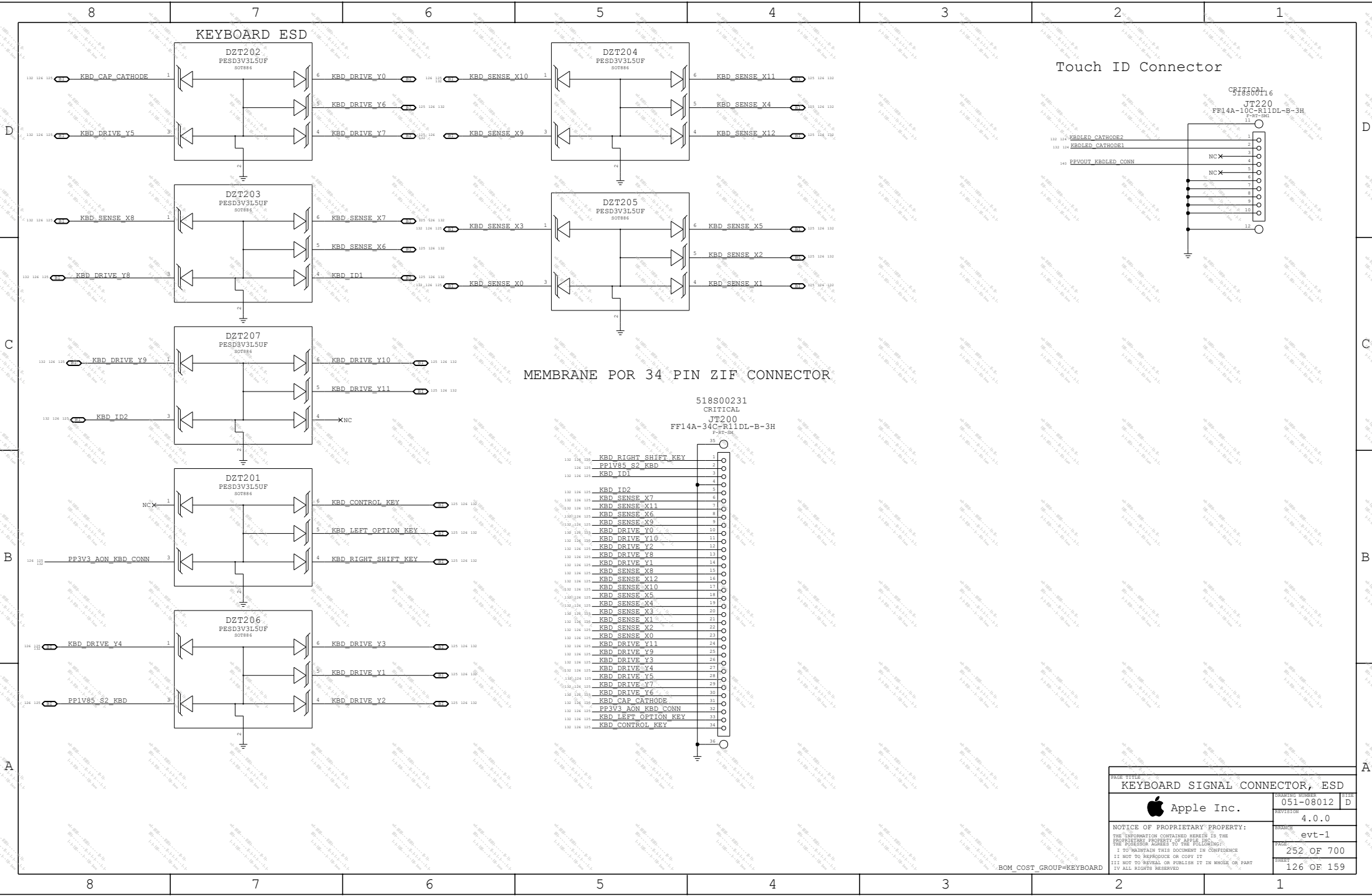
KEYBOARD SWITCH NODE DESENSE OPTION					
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131800141	1	CAP,ORG,129F,5K,100V,0201	CT013		BLC KBD SW NODE DESENSE

PAGE TITLE		BEN: KEYBD BKLT	
 Apple Inc.	FILE NO.	051-08012	PAGE 1
	REVISION	4.0.0	
	DESCRIPTION	evt-1	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF APPLE INC.			
TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 1) NOT TO REPRODUCE OR COPY IT 2) NOT TO DISSEMINATE OR CITE IT 3) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART TO ANY OTHER PERSON OR ENTITY	FILE NO.	050 OF 700	
	PAGE	124	OF 159



PART NUMBER	ALTERNATE FOR PART NUMBER	HOW OPTION	REF DES	COMMENTS
353800879	353800754	ANY	ALL	ESDKit//32477358

PAGE TITLE			
KEYBOARD IOX, SUPPORT			
	Apple Inc.		051-08012
			4.0.0
NOTICE OF PROPRIETARY PROPERTY:		evt-1	
THIS INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY FORM OR BY ANY MEANS WITHOUT THE EXPRESS WRITTEN PERMISSION OF APPLE INC.		251 OF 700	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		125 OF 159	
IT NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IN ALL RIGHTS RESERVED			



PAGE TITLE		
KEYBOARD SIGNAL CONNECTOR, ESD		
	051-08012	D
	4.0.0	
NOTICE OF PROPRIETARY PROPERTY:		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE RECIPIENT AGREES TO THE FOLLOWING:		
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		
I NOT TO REPRODUCE OR COPY IT		
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		
I TO ALL RIGHTS RESERVED		
252 OF 700	126 OF 159	

BOM_COST_GROUP=KEYBOARD

TRACKPAD SPI BUS LEVEL SHIFTER

RSVD LS

PMU CLK LS

TOUCH INTERRUPT LS

TOUCH CS LS

MCU INTERRUPT LS

SWD LEVEL SHIFTERS

Temp Sensor I2C Level Shifter

SN74AVC4T774 Truth Table

CTRL INPUTS		OUTPUT CIRCUITS		OPERATION
/OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

SYS AWAKE LS

TRACKPAD/KEYBOARD WAKE LS

TABLE 1: SMC I2C3

DEVICE	CARD/REFDES	7-BIT	8-BIT	SPEED
Palm Rest Temp	IPD	0X4C	0X98	100KHZ

TABLE 2: TRACKPAD SUPPORT 1

REVISION	DATE	DESCRIPTION
051-08012		
4.0.0		

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE EXPRESS WRITTEN PERMISSION OF APPLE INC.

Apple Inc.

253 OF 700

127 OF 159

CTRL INPUTS		OUTPUT CIRCUITS		OPERATION
/OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

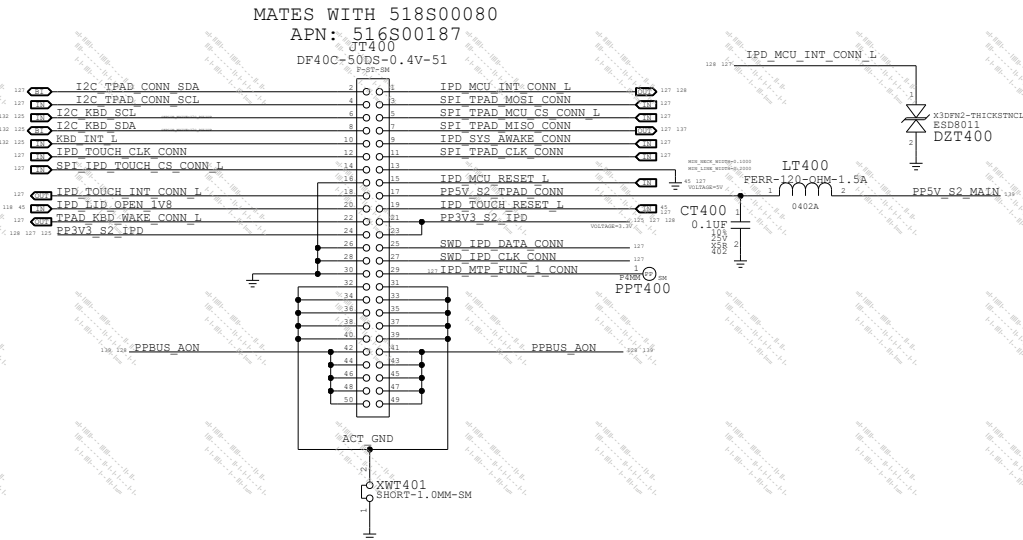
[illegible]

The schematic diagram illustrates the RESET PULL-UPS circuit for the UT380 LSF0101R7. Key components and connections include:

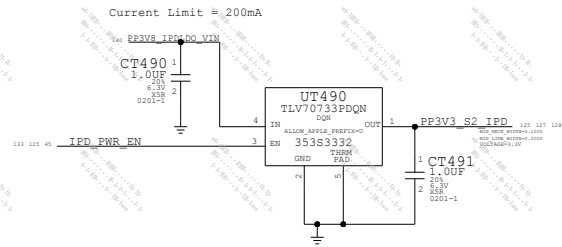
- Power Regulation:** Two 3.3V regulators are shown: PF1V2_S2 and PF3V3_S2_IPD. Both are configured with BOMPTION=DEV_IPD. Decoupling capacitors RT380 (47K, 0.1uF), RT381 (200K, 0.1uF), and RT385 (200K, 0.1uF) are used for filtering.
- USB-to-UART Bridge:** A CP2102 bridge is connected to the SWD_NUB_IPD_SWDIO pin of the UT380. It is powered by the 3.3V regulator (PF3V3_S2_IPD) and has its ground connected to the SWD_IPD_DATA_CONN pin.
- UT380 LSF0101R7:** The microcontroller is shown with pins VREF_A, VREF_B, VDDA, and VDDIO. It is connected to the SWD_IPD_DATA_CONN pin and has a GND connection.
- Configuration:** The BOMPTION=DEV_IPD setting is noted for the regulators and the microcontroller.

DEVICE	CARD/REFDES	7-BIT	8-BIT	SPEED
Palm Rest Temp	IPD	0X4C	0X98	100KHZ

PART 1		TRACKPAD SUPPORT 1
Apple Inc.	CREATING NUMBER	051-08012
	REVISION	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND THE RECIPIENT AGREES TO THE FOLLOWING: THE RECIPIENT AGREES TO CONFIDENTIALITY OF THE INFORMATION AND TO: 1. NOT TO REPRODUCE OR COPY IT 2. NOT TO DISCLOSE OR PUBLISH IT IN WHOLE OR PART 3. NOT TO TRANSFER IT TO ANY OTHER PARTY	ISSUE	evt-1
	PAGE	253 OF 700
TRACKPAD SUPPORT 1		127 OF 158



3.3V LDO (LOCAL TO IPD)



PAGE TITLE		
TRACKPAD SUPPORT 2		
Apple Inc.	051-08012	PAGE D
	4.0.0	
NOTICE OF PROPRIETARY PROPERTY:		REVISION
THE INFORMATION CONTAINED HEREIN IS THE		evt-1
PROPRIETARY PROPERTY OF APPLE INC.		254 OF 700
THE REVISION AGREES TO THE FOLLOWING:		128 OF 159
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		
I NOT TO REPRODUCE OR COPY IT		
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		
I TO ALL RIGHTS RESERVED		

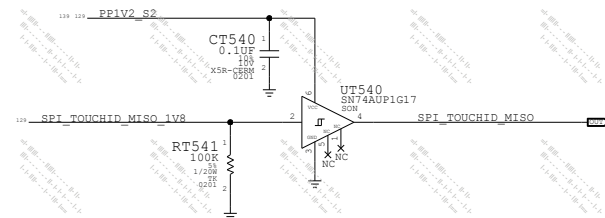
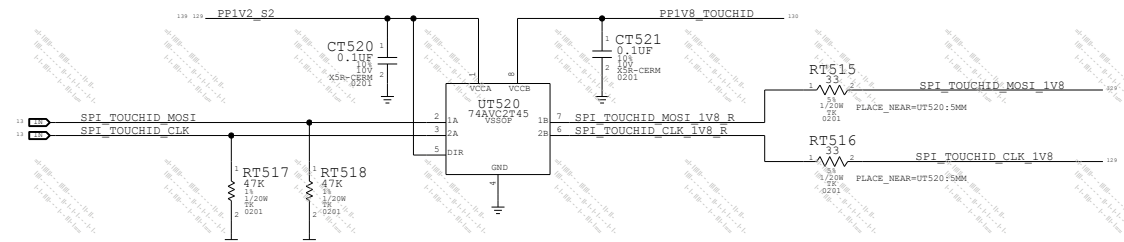
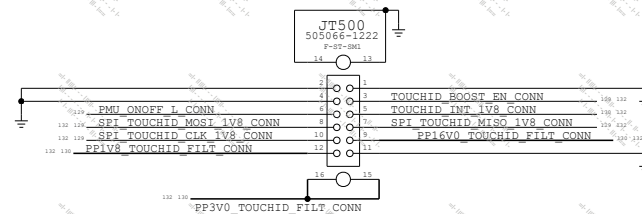
BOM_COST_GROUP=TRACPAD

THIS PAGE FOR REFERENCE ONLY - COPY ONCE, SYNC ONLY AS NEEDED

The diagram illustrates the PCB layout for the SPI and TOUCHID interfaces. It shows the placement of capacitors and resistors for the following connections:

- PMU_ONOFF_L_CONN**: Connected to **RT504** (117s00073) and **CT504** (100PF).
- SPI_TOUCHID_CLK_Iv8_CONN**: Connected to **RT570** (117s00073) and **CT572** (56PF).
- SPI_TOUCHID_MOSI_Iv8_CONN**: Connected to **RT580** (117s00073) and **CT582** (56PF).
- SPI_TOUCHID_MISO_Iv8_CONN**: Connected to **RT540** (117s00073) and **CT541** (56PF).
- TOUCHID_BOOST_EN_CONN**: Connected to **RT503** (117s00073) and **CT503** (100PF).

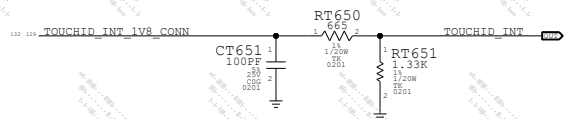
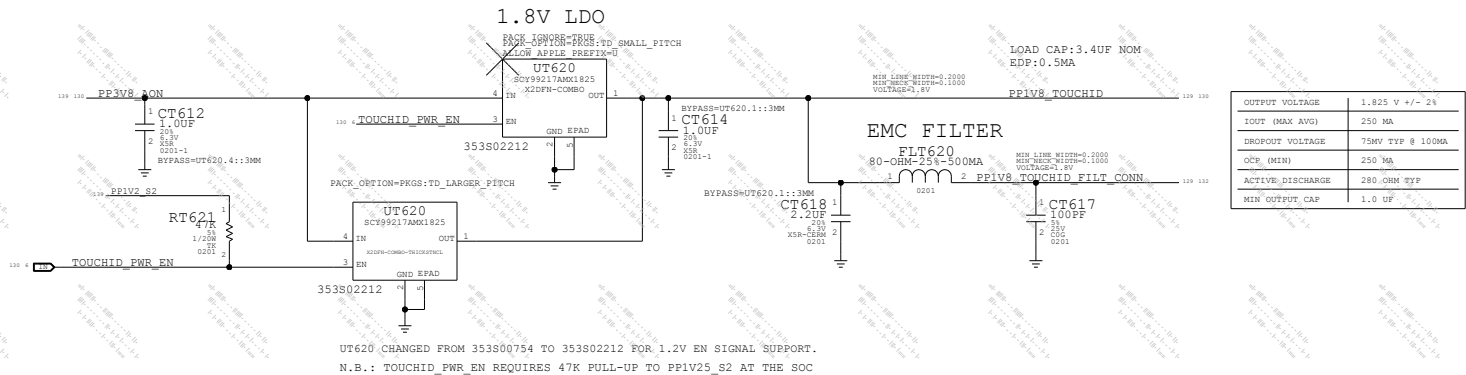
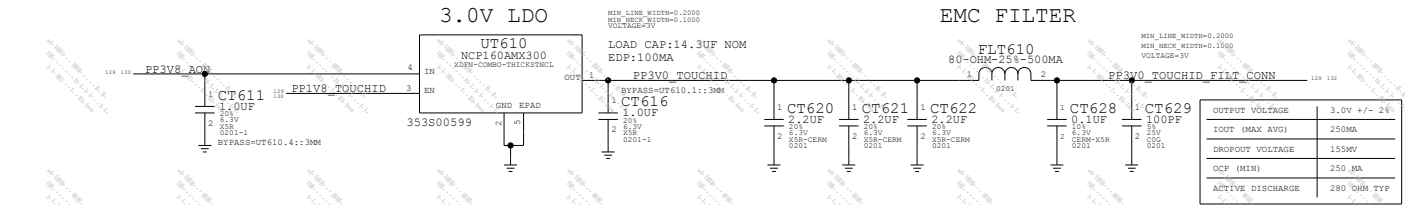
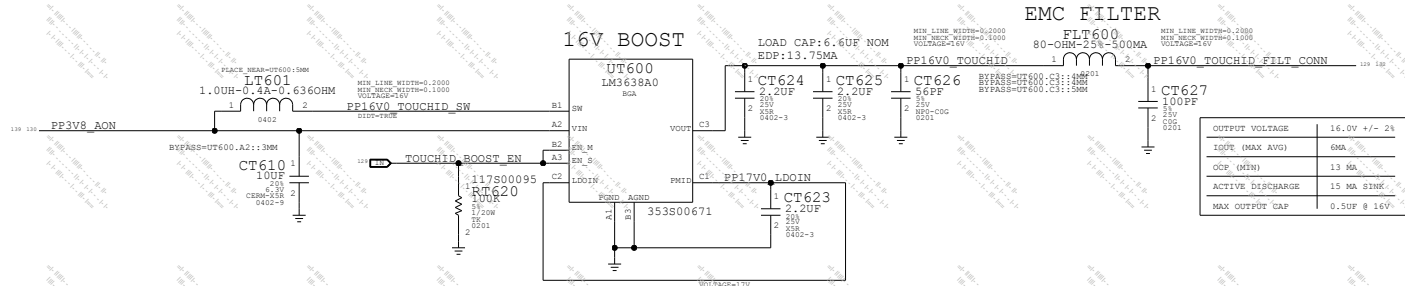
The layout also shows the placement of the capacitors and resistors for the **SPI_TOUCHID_CLK_Iv8_CONN**, **SPI_TOUCHID_MOSI_Iv8_CONN**, **SPI_TOUCHID_MISO_Iv8_CONN**, and **TOUCHID_BOOST_EN_CONN** connections.



DOC NUMBER		
PAGE TITLE		
TOUCHID CONN		
 Apple Inc.	051-08012	NEW
	REVISION	
	4.0.0	
	DRAFT	
	evt-1	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.		
1. TO MAINTAIN THIS DOCUMENT IN CONFIDENTIALITY 2. TO MAINTAIN THE CONFIDENTIALITY OF THE INFORMATION CONTAINED HEREIN 3. TO NOT REVEAL OR DISCLOSE IN WHOLE OR PART TO ANY OTHER PERSON OR ENTITY		
255 OF 700		
129 OF 159		

*** OK2INTEGRATE ***

TOUCHID POWER SEQUENCING REQUIREMENTS
POWER ON: 1V8 -> 3V3 -> 16V0



BOB_COST_GROUP=TOUCHID

TOUCHID SUPPORT		
Apple Inc.	051-08012	Page D
	4.0.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE RECIPIENT AGREES TO THE FOLLOWING: 1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2. NOT TO REPRODUCE OR COPY IT 3. NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IN ANY MANNER	evt-1	
	256 OF 700	
	130 OF 159	

NAND0 TEST POINTS

104 103 102 101 100	NAND0_LPB_L	TPU603	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_BFH	TPU604	TP-P4
103 102 101 100	NAND0_BOOT2	TPU605	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E0_SWD_UID0	TPU606	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E1_SWD_UID0	TPU607	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E2_SWD_UID0	TPU608	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E3_SWD_UID0	TPU609	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E0_SWD_UID1	TPU610	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E1_SWD_UID1	TPU611	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E2_SWD_UID1	TPU612	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E3_SWD_UID1	TPU613	TP-P4
104 103 102 101 100	NAND0_PFN_L	TPU614	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_PCIE_RESET_L	TPU615	TP-P4
100 107 106 105 104 103 102 101 100	SWD_NAND0_SWDIO	TPU616	TP-P4
100 107 106 105 104 103 102 101 100	SWD_NAND0_SWCLK	TPU617	TP-P4
103 102 101 100	NAND0_WP_L	TPU618	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_CLKREQ0_L	TPU619	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_CLKREQ1_L	TPU620	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_CLKREQ2_L	TPU621	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_CLKREQ3_L	TPU622	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E0_PCIE_RESREF	TPU623	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E1_PCIE_RESREF	TPU624	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E2_PCIE_RESREF	TPU625	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E3_PCIE_RESREF	TPU626	TP-P4
104 103 102 101 100	NAND0_RESET_L	TPU627	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E2_ZO_0	TPU632	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_S5E2_ZO_1	TPU633	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_S5E0_JTAG_TDI	TPU668	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_S5E3_JTAG_TDO	TPU669	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_JTAG_SEL	TPU670	TP-P4
100 107 106 105 104 103 102 101 100	NAND0_JTAG_TRST_L	TPU671	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_S5E0_ANI1_VREF	TPU672	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_S5E0_ANI0_VREF	TPU673	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_S5E1_ANI1_VREF	TPU674	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_S5E1_ANI0_VREF	TPU675	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_S5E2_ANI1_VREF	TPU676	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_S5E2_ANI0_VREF	TPU677	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_S5E3_ANI1_VREF	TPU678	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_S5E3_ANI0_VREF	TPU679	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E2_ANI1_VREF	TPU690	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E2_ANI0_VREF	TPU691	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E3_ANI1_VREF	TPU692	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E3_ANI0_VREF	TPU693	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_OCARINA_VEN2	TPU600	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_OCARINA_VEN2	TPU601	TP-P4

NAND1 TEST POINTS

100 107 106 105 104 103 102 101 100	NAND1_LPB_L	TPU636	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_BOOT2	TPU637	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E0_SWD_UID0	TPU638	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E1_SWD_UID0	TPU639	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E2_SWD_UID0	TPU640	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E3_SWD_UID0	TPU641	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E0_SWD_UID1	TPU642	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E1_SWD_UID1	TPU643	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E2_SWD_UID1	TPU644	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E3_SWD_UID1	TPU645	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_PFN_L	TPU646	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_PCIE_RESET_L	TPU647	TP-P4
100 107 106 105 104 103 102 101 100	SWD_NAND1_SWDIO	TPU648	TP-P4
100 107 106 105 104 103 102 101 100	SWD_NAND1_SWCLK	TPU649	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_WP_L	TPU650	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_CLKREQ0_L	TPU651	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_CLKREQ1_L	TPU652	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_CLKREQ2_L	TPU653	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_CLKREQ3_L	TPU654	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E0_PCIE_RESREF	TPU655	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E1_PCIE_RESREF	TPU656	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E2_PCIE_RESREF	TPU657	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E3_PCIE_RESREF	TPU658	TP-P4
104 103 102 101 100	NAND1_RESET_L	TPU659	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E1_ZO_1	TPU662	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E2_ZO_0	TPU664	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E2_ZO_1	TPU665	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E1_JTAG_TDO	TPU680	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_S5E2_JTAG_TDO	TPU681	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E0_JTAG_TDI	TPU682	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E3_JTAG_TDO	TPU683	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_JTAG_SEL	TPU684	TP-P4
100 107 106 105 104 103 102 101 100	NAND1_JTAG_TRST_L	TPU685	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E0_ANI1_VREF	TPU686	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E0_ANI0_VREF	TPU687	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E1_ANI1_VREF	TPU688	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E1_ANI0_VREF	TPU689	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E2_ANI1_VREF	TPU690	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E2_ANI0_VREF	TPU691	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E3_ANI1_VREF	TPU692	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_S5E3_ANI0_VREF	TPU693	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND0_OCARINA_VEN2	TPU600	TP-P4
100 107 106 105 104 103 102 101 100	TP_NAND1_OCARINA_VEN2	TPU601	TP-P4

TEST POINTS REQUESTED BY AUDIO TEAM

110 109 108 107 106 105 104 103 102 101 100	PP3V8_CODEC_VP	TPU6B0	TP-P4
110 109 108 107 106 105 104 103 102 101 100	PP1V8_CODEC_VCP	TPU6B1	TP-P4
110 109 108 107 106 105 104 103 102 101 100	CODEC_RESET_L	TPU6B2	TP-P4
110 109 108 107 106 105 104 103 102 101 100	CODEC_INT_L	TPU6B_3	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TDM_CODEC_FSYNC	TPU6B4	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TDM_CODEC_R2D	TPU6B5	TP-P4
110 109 108 107 106 105 104 103 102 101 100	PLACE_NEAR=U0600.B055:300M TDM_CODEC_D2R	TPU6B6	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TDM_CODEC_BCLK	TPU6B7	TP-P4
110 109 108 107 106 105 104 103 102 101 100	I2C_CODEC_SDA	TPU6B8	TP-P4
110 109 108 107 106 105 104 103 102 101 100	I2C_CODEC_SCL	TPU6B9	TP-P4
110 109 108 107 106 105 104 103 102 101 100	SPKRAMP_RESET_L	TPU6E0	TP-P4
110 109 108 107 106 105 104 103 102 101 100	SPKRAMP_INT_L	TPU6E1	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TDM_SPKRAMP_L_BCLK	TPU6E2	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TDM_SPKRAMP_L_FSYNC	TPU6E3	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TDM_SPKRAMP_L_R2D	TPU6E4	TP-P4
110 109 108 107 106 105 104 103 102 101 100	PLACE_NEAR=U0600.B055:200M TDM_SPKRAMP_L_D2R	TPU6E5	TP-P4
110 109 108 107 106 105 104 103 102 101 100	SPKRAMP_ICC	TPU6E6	TP-P4
110 109 108 107 106 105 104 103 102 101 100	I2C_SPKRAMP_L_SCL	TPU6E7	TP-P4
110 109 108 107 106 105 104 103 102 101 100	I2C_SPKRAMP_L_SDA	TPU6E8	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TP_SPKRAMP_A_IV_EN	TPU6E9	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TP_SPKRAMP_B_IV_EN	TPU6F0	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TP_SPKRAMP_C_IV_EN	TPU6F1	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TDM_SPKRAMP_R_BCLK	TPU6F2	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TDM_SPKRAMP_R_FSYNC	TPU6F3	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TDM_SPKRAMP_R_R2D	TPU6F4	TP-P4
110 109 108 107 106 105 104 103 102 101 100	PLACE_NEAR=U0600.BD50:200M TDM_SPKRAMP_R_D2R	TPU6F5	TP-P4
110 109 108 107 106 105 104 103 102 101 100	I2C_SPKRAMP_R_SCL	TPU6F6	TP-P4
110 109 108 107 106 105 104 103 102 101 100	I2C_SPKRAMP_R_SDA	TPU6F7	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TP_SPKRAMP_D_IV_EN	TPU6F8	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TP_SPKRAMP_E_IV_EN	TPU6F9	TP-P4
110 109 108 107 106 105 104 103 102 101 100	TP_SPKRAMP_F_IV_EN	TPU6A6	TP-P4
110 109 108 107 106 105 104 103 102 101 100	PPM_DMIC_DATA0	TPU6G8	TP-P4
110 109 108 107 106 105 104 103 102 101 100	PPM_DMIC_DATA1	TPU6G9	TP-P4
110 109 108 107 106 105 104 103 102 101 100	PLACE_NEAR=U0600.BD11:200M		
110 109 108 107 106 105 104 103 102 101 100	CODEC_WAKE_L	TRUE	46 110

SGA MISC DEBUG TEST-POINTS

45 10	PLACE_SIDE=BOTTOM PMU_CLK32K_SOC	TPU6C6	TP-P4
10	PLACE_SIDE=TOP TPT_SOC_DOCK_ATTENTION	TPU6C7	TP-P4
10	PLACE_SIDE=BOTTOM TPT_AON_SLEEP1_RESET_L	TPU6C8	TP-P4
130 131 10	PLACE_SIDE=BOTTOM SMC_FIXTURE_MODE_L	TPU6C9	TP-P4
10	SOC_JTAG_SEL	TPU6D0	TP-P4
130 73 11	SWD_SOC_SWCLK	TPU6D1	TP-P4
140 10	SOC_JTAG_TDI	TPU6D2	TP-P4
140 10	SOC_JTAG_TDO	TPU6D3	TP-P4
130 73 11	SWD_SOC_SWDIO	TPU6D4	TP-P4
10	TPT_JTAG_SOC_TRST_L	TPU6D5	TP-P4

SGA JTAG TEST-POINTS

SGA DEBUG TEST-POINTS

145 0	EUSB_ATCO_P	PPU610	TP-P4
145 0	EUSB_ATCO_N	PPU611	TP-P4
145 0	EUSB_ATCO_N	PPU612	TP-P4
145 0	EUSB_ATCO_N	PPU613	TP-P4
145 0	EUSB_ATC1_P	PPU614	TP-P4
145 0	EUSB_ATC1_N	PPU615	TP-P4
145 0	EUSB_ATC1_N	PPU616	TP-P4
145 0	EUSB_ATC1_N	PPU617	TP-P4
145 0	EUSB_ATC2_P	PPU618	TP-P4
145 0	EUSB_ATC2_N	PPU619	TP-P4
145 0	EUSB_ATC2_N	PPU620	TP-P4
145 0	EUSB_ATC2_N	PPU621	TP-P4
145 0	EUSB_DBG_P	PPU623	TP-P4
145 0	EUSB_DBG_N	PPU625	TP-P4
145 0	EUSB_DBG_P	PPU626	TP-P4
145 0	EUSB_DBG_N	PPU627	TP-P4
145 0	EUSB_DBG_P	PPU628	TP-P4
145 0	EUSB_DBG_N	PPU629	TP-P4
145 0	EUSB_DBG_P	PPU62A	TP-P4
145 0	EUSB_DBG_N	PPU62B	TP-P4

PAGE TITLE			
ICT/FCT-1			
Apple Inc.		051-08012	D
NOTICE OF PROPRIETARY PROPERTY:		4.0.0	
THE INFORMATION CONTAINED HEREIN IS THE		evt-1	
PROPRIETARY PROPERTY OF APPLE INC.		266 OF 700	
THE INFORMATION CONTAINED HEREIN IS THE		131 OF 159	
PROPRIETARY PROPERTY OF APPLE INC.			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
I NOT TO REPRODUCE OR COPY IT			
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			

USBC Debug 3mm PPs

PPU8C7
P3MM TP_PPHV_INT0_AONSW 33 72
PPU8C0
P3MM TP_PPHV_INT1_AONSW 33 72
PPU8C6
P3MM TP_PPHV_INT2_AONSW 33 81

USB2 DEBUG PPs

PPU800
P3MM TP_MACAW0_DEBUG_SWDCCLK 72 74
PPU801
P3MM TP_MACAW0_DEBUG_SWDDAT 72 74
PPU802
P3MM TP_MACAW1_DEBUG_SWDCCLK 72 82
PPU803
P3MM TP_MACAW1_DEBUG_SWDDAT 72 74
PPU804
P3MM TP_MACAW2_DEBUG_SWDCCLK 44
PPU805
P3MM TP_MACAW2_DEBUG_SWDDAT 44

AUSTRINTGER PPs rdar://79988718

PPU810
P2MM P1V8VDDH_PWR_EN_R 48
PPU811
P2MM P1V8VDDH_SLP_R_L 48
PPU813
P2MM P1V8VDDH_ILIMIT_THROTTLE_L 5 48 133
PPU814
P2MM P1V8VDDH_TLIMIT_THROTTLE_L 5 48 133
PPU817
P3MM P1V8VDDH_IMON 48
PPU818
P3MM P1V8VDDH_IMON_FILT 48
PPU819
P3MM P1V8VDDH_IREF_R 48 48 50
PPU820
P3MM P1V8VDDH_DRMOS_FAULT_L 47 48 48 50
PPU821
P3MM P1V8VDDH_DRMOS_EN 47 48 48 50
PPU822
P2MM P1V8VDDH_DRMOS_FWM1 47 48 48
PPU823
P2MM P1V8VDDH_DRMOS_FWM2 47 48 48
PPU824
P2MM P1V8VDDH_DRMOS_FWM3 47 48 48
PPU825
P2MM P1V8VDDH_DRMOS_FWM4 47 48
PPU826
P2MM P1V8VDDH_DRMOS_FWM5 47 48
PPU827
P3MM P1V8VDDH_SEM_L 48 48 50

AUSTRINTGER PPs

PP1V8_S1_CLVR_VDDH 141
OMIT PPU890 TP-5016
OMIT PPU891 TP-5016
OMIT PPU892 TP-5016
OMIT PPU893 TP-5016

NO TESTS

PPVDD_PCPU_AWAKESW NO TEST 141
PPVDD_PCPU_AWAKESW NO TEST 141

PPVDD_FIXED_S1_DCS_0 NO TEST 20
PPVDD_FIXED_S1_DCS_2 NO TEST 20
PPVDD_FIXED_S1_DDR_0 NO TEST 20
PPVDD_FIXED_S1_DDR_2 NO TEST 20
PP1V2_S2_AOP0_S2 NO TEST 21

PPVDD_GPU_SRAM0_AWAKESW NO TEST 11 133 141
PPVDD_GPU_SRAM1_AWAKESW NO TEST 11 133 141
PPVDD_PCPU_SRAM0_AWAKESW NO TEST 11 133 141
PPVDD_PCPU_SRAM1_AWAKESW NO TEST 11 133 141

PPVDD_PCPU_SRAM0_AWAKESW NO TEST 11 133 141
PP1V2_S2_ULPPLL NO TEST 21
PP1V2_AWAKE_C2C NO TEST 21
PPVDD_LOW_S2_ULPPLL NO TEST 16
PPVDD_LOW_S2_FIEPLL NO TEST 21
PP1V2_AWAKE_PCIE_PIL NO TEST 21
PPVDD_FIXED_S1_PCIE_PL_0P_0P NO TEST 20
PPVDD_FIXED_S1_PCIE_PIL NO TEST 20
PPVDD_PCPU_SRAM1_AWAKESW NO TEST 11 133 141
PPVDD_FABRIC_S1 NO TEST 141

PPVDD_GPU_AWAKESW NO TEST 11 141
PPVDD_ANE_SRAM_AWAKESW NO TEST 11 141
PPVDD_ANE_AWAKESW NO TEST 141

PP1V2_AWAKE_GRP0 NO TEST 21
PPVDD_GPU0_AWAKESW NO TEST 141
PP1V2_AWAKE_GRP1 NO TEST 21
PP1V2_AWAKE_FMON NO TEST 21

PCIE_WLBT_R2D_P NO TEST 98
PCIE_WLBT_R2D_N NO TEST 98
PCIE_WLBT_D2R_C_P NO TEST 98
PCIE_WLBT_D2R_C_N NO TEST 98

NO TESTS SGPIO/MPMU/SPMU

- NO-TEST added to prevent PAL from placing test vias.
- Characterization probe access is desired within 50mm of any input pin.
- We can use the series/branch resistor pads to probe, if they are within that distance.
- After PAL routes the board, we will check this 50mm-access and modify NO-TEST as needed per signal to add test vias

SGPIO_FMU_SPMU_CLK_R NO TEST 44 45
SGPIO_FMU_CLVR_CLK_R NO TEST 44 45
SGPIO_FMU_DATA_R NO TEST 44 45
SGPIO_FMU_CLVR_CLK NO TEST 45
SGPIO_FMU_DATA NO TEST 45

SGPIO_FMU_SPMU_CLK NO TEST property per David T

SGPIO_FMU_CLVR0_CLK NO TEST 45 51
SGPIO_FMU_CLVR1_CLK NO TEST 45 51
SGPIO_FMU_CLVR2_CLK NO TEST 45 51
SGPIO_FMU_CLVR0_DATA NO TEST 45 51
SGPIO_FMU_CLVR1_DATA NO TEST 45 51
SGPIO_FMU_CLVR2_DATA NO TEST 45 51
SGPIO_FMU_SPMU_DATA NO TEST 45 45

SPMI_CLVR0_CLK NO TEST 11 51
SPMI_CLVR0_DATA_R NO TEST 11 51
SPMI_CLVR1_CLK NO TEST 11 51
SPMI_CLVR1_DATA_R NO TEST 11 51
SPMI_CLVR2_CLK NO TEST 11 51
SPMI_CLVR2_DATA_R NO TEST 11 51
SPMI_CLVR0_CLK_R NO TEST 5 48
SPMI_CLVR1_CLK_R NO TEST 5 48
SPMI_CLVR2_CLK_R NO TEST 5 48
SPMI_CLVR0_DATA NO TEST 11 51
SPMI_CLVR1_DATA NO TEST 11 51
SPMI_CLVR2_DATA NO TEST 11 51

SPMI_NUB_MPMU_CLK NO TEST 11 44
SPMI_NUB_MPMU_DATA NO TEST 11 44
SPMI_NUB_MPMU_CLK_R NO TEST 11 44
SPMI_NUB_MPMU_DATA_R NO TEST 11 44

SPMI_NUB_SPMU_CLK NO TEST 11 40
SPMI_NUB_SPMU_DATA NO TEST 11 40
SPMI_NUB_P1V8VDDH_CLK NO TEST 11 48
SPMI_NUB_P1V8VDDH_DATA NO TEST 11 48

SPMI_NUB_SPMU_P1V8VDDH_CLK NO TEST 11
SPMI_NUB_SPMU_P1V8VDDH_DATA_R NO TEST 11 51
SPMI_NUB_SPMU_P1V8VDDH_DATA NO TEST 11
SPMI_NUB_SPMU_P1V8VDDH_CLK_R NO TEST 11 11

Power Sequencing PPs

PPU8A1 GND_SEMU_QUIET 40
PPU8A2 GND_MPMU_QUIET 44
PPU8A3 PMU_CRASH_L 44 45
PPU8A5 DBL_CLICK_DET 4 44
PPU8A6 P5VS2_PWR_EN 44 45
TPU8A7 P5VS2TPS_PWR_EN 45 52 146
PPU8A8 P5VS2SN_PG00D 52 146
PPU8A9 IPD_PWR_HOLD 40 45
PPU8B0 IPD_PWR_EN 45 123 128
PPU8B1 IPD_PWR_EN_PMU 45
PPU8B2 PMU_SCRASH_L 45 45
PPU8B3 P1V8VDDH_SLP_L 45 48 128
PPU8B4 P1V8VDDH_PWR_EN 44 45 48
PPU8B5 CLVR_RESET_L 44 51 52 53
PPU8B6 P3V8AON_LPM 14 45
PPU8B7 P3V8AON_PWR_EN 19 29 30 34
TPU8B8 CHGR_AUX_OK 40 45

PPU8C1 P1V8VDDH_ILIMIT_THROTTLE_L 5 48 133
PPU8C2 P1V8VDDH_TLIMIT_THROTTLE_L 5 48 133
PPU8C3 PMU_UVWARN_ILIMIT_L 5 11
PPU8C4 EDP_BKLT_IV29_EN 45 114
PPU8C5 UPC_PMU_RESET_IV2 44 45

SI PP

PPU8E1 SPT_DISP_BKLT_MISO 7 114 110

PPU830 TPT_AP_UART2_R2D 4 145
PPU831 TPT_AP_UART2_D2R 4 145
PPU832 TPT_AP_UART2_R2D_RTS_L 4 145
PPU833 TPT_AP_UART2_D2R_CTS_L 4 145

PMU Serial PPs for characterization

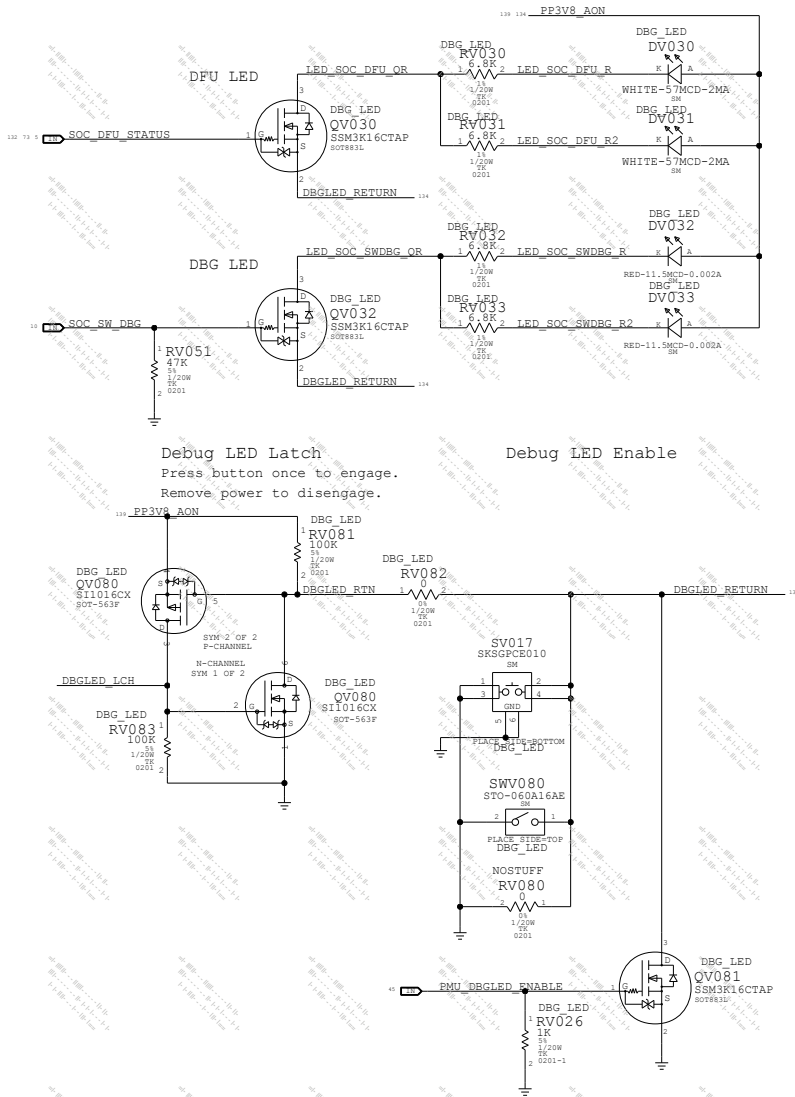
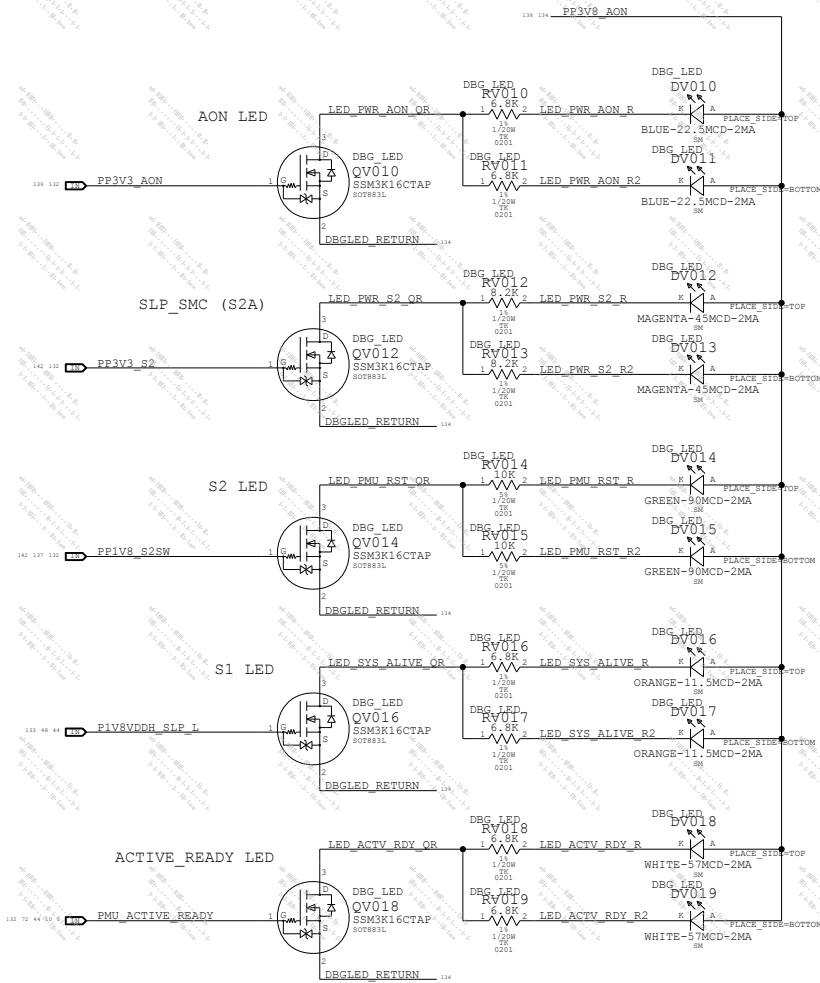
Other PMU serial data are accessible to probe within 50mm of their SR, on their series 2 pads or test via

removed

SPMU/MPMU PPs HAVE MOVED TO PROJECT CSAs

PMU AND OTHER TEST POINTS			
Apple Inc.		051-08012	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. NO REPRODUCTION OR DISSEMINATION IS PERMITTED WITHOUT THE WRITTEN AGREEMENT OF THE REPRODUCING PARTY.		4.0.0	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		evt-1	
268 OF 700		133 OF 159	

Debug LEDs



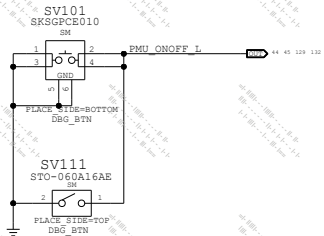
Debug: LEDs, Koba	
Apple Inc.	051-08012
NOTICE OF PROPRIETARY PROPERTY:	4.0.0
THE INFORMATION CONTAINED HEREIN IS THE	evt-1
PROPRIETARY PROPERTY OF APPLE INC.	270 OF 700
ONE SHOULD NOT REPRODUCE OR COPY IT	134 OF 159
WITHOUT THE WRITTEN PERMISSION OF APPLE INC.	

BOM_COST_GROUP=DEBUG

POWER BUTTON

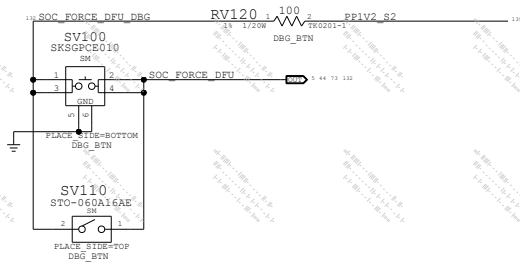
Imitate a user-facing Power Button press, many functions:

- Press to Wake from any state
- Combine with RSLOC (see RSLOC)
- Hold for 8sec to trigger "one-finger reset"
- - Similar to PMU RESET, except SW gets a warning to initiate panic-flow



FORCE DFU

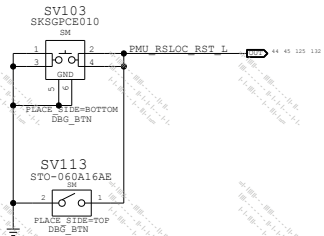
Hold during OFF->AWAKE transition to enter SOC's "Debug Firmware Update" mode



RSLOC BUTTON

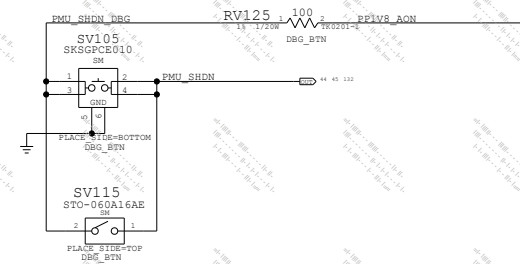
Imitate a user-facing key combo Right-Shift + Left-Option + Control:

- Hold RSLOC 4sec, then press Power Button to initiate PMU RESET
- Hold RSLOC 4sec, then hold Power Button 4sec to power-cycle P3V8AON VR
- Hold Power Button 1sec, then hold RSLOC 10sec to trigger PMU RESET into DFU (continue holding first button when second button is added)



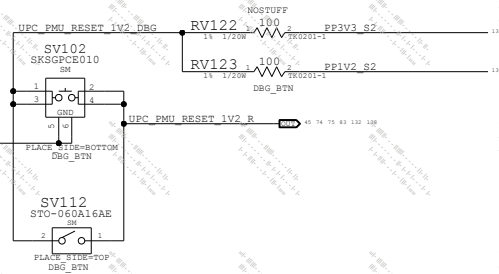
PMU SHUTDOWN

PMU transitions to OFF state and stays there while this is asserted, then waits for a WAKE source* to boot



PMU RESET

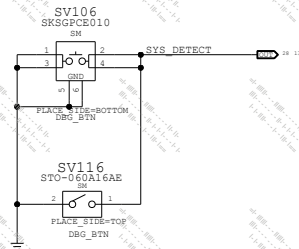
PMU transitions to OFF and automatically proceeds up to AWAKE



SYS_DETECT (Battery Disconnect)

Imitate unplugging the battery signal flex, to disconnect MLB from Battery power

- Disconnect all DCIN sources, then hold SYS_DETECT for 30sec*. MLB will completely power down
- *Time depends on 3V8AON and PBUS decay rate, and should be quantified in system

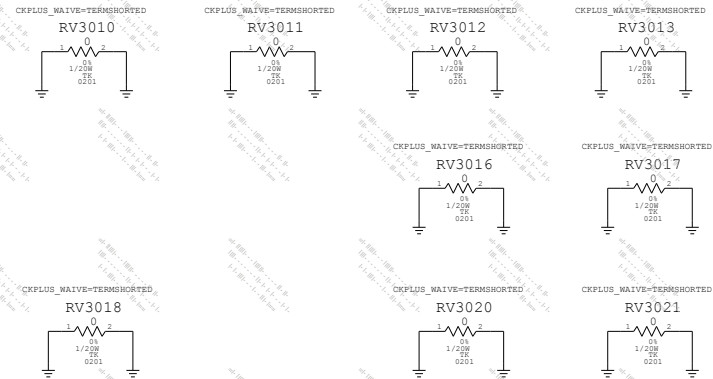


*WAKE sources in OFF:
CHGR_AUX_OK (DCIN present)
IPD_LID_OPEN_IV8 (Lid is open)
PMU_ONOFF_L (User Power Button)

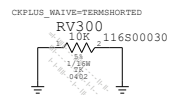
Page Title			
Debug: Buttons			
 Apple Inc.	051-08012	DATE	D
	4.0.0	REVISION	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE REVISIONS AGREE TO THE FOLLOWING:			
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
11 NOT TO REPRODUCE OR COPY IT			
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
1111 ALL RIGHTS RESERVED			
271 OF 700			135 OF 159

BOM_COST_GROUP=DEBUG

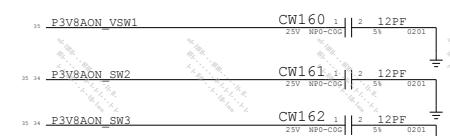
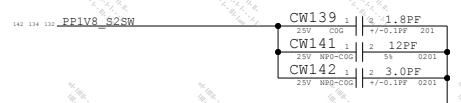
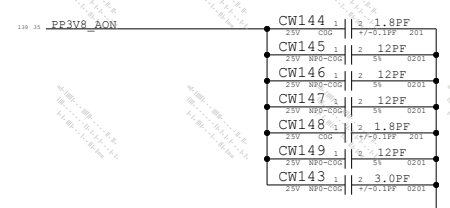
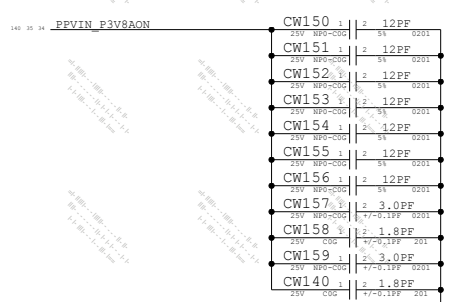
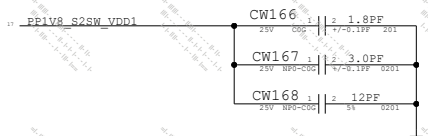
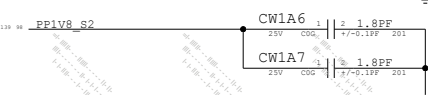
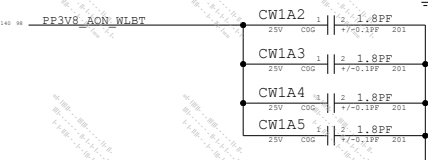
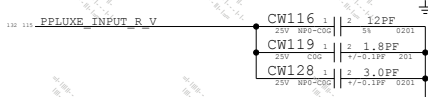
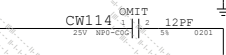
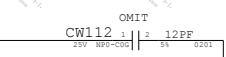
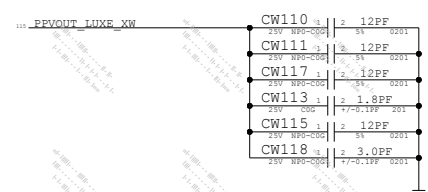
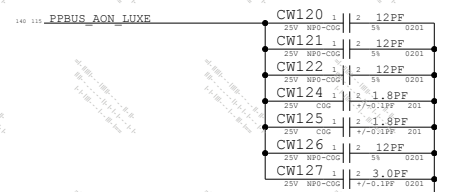
NAND ASSEMBLY PROTECTION PURPOSES



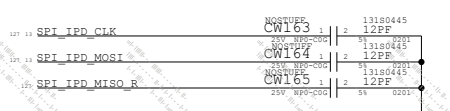
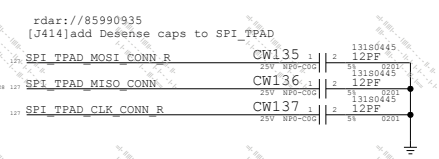
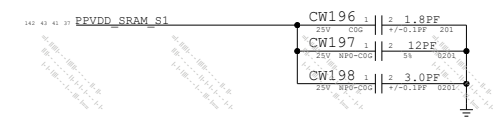
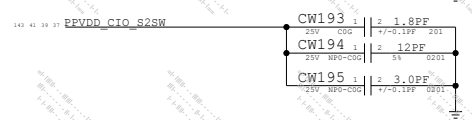
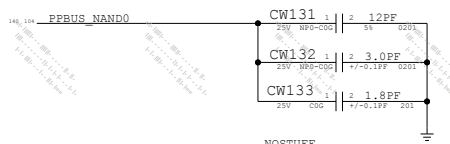
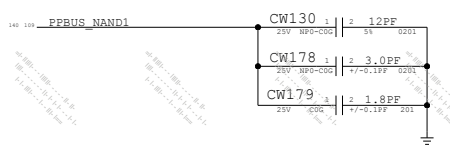
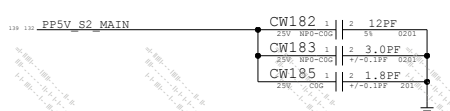
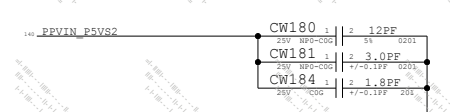
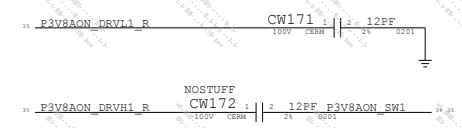
FOR ASSEMBLY PROTECTION PURPOSES ONLY



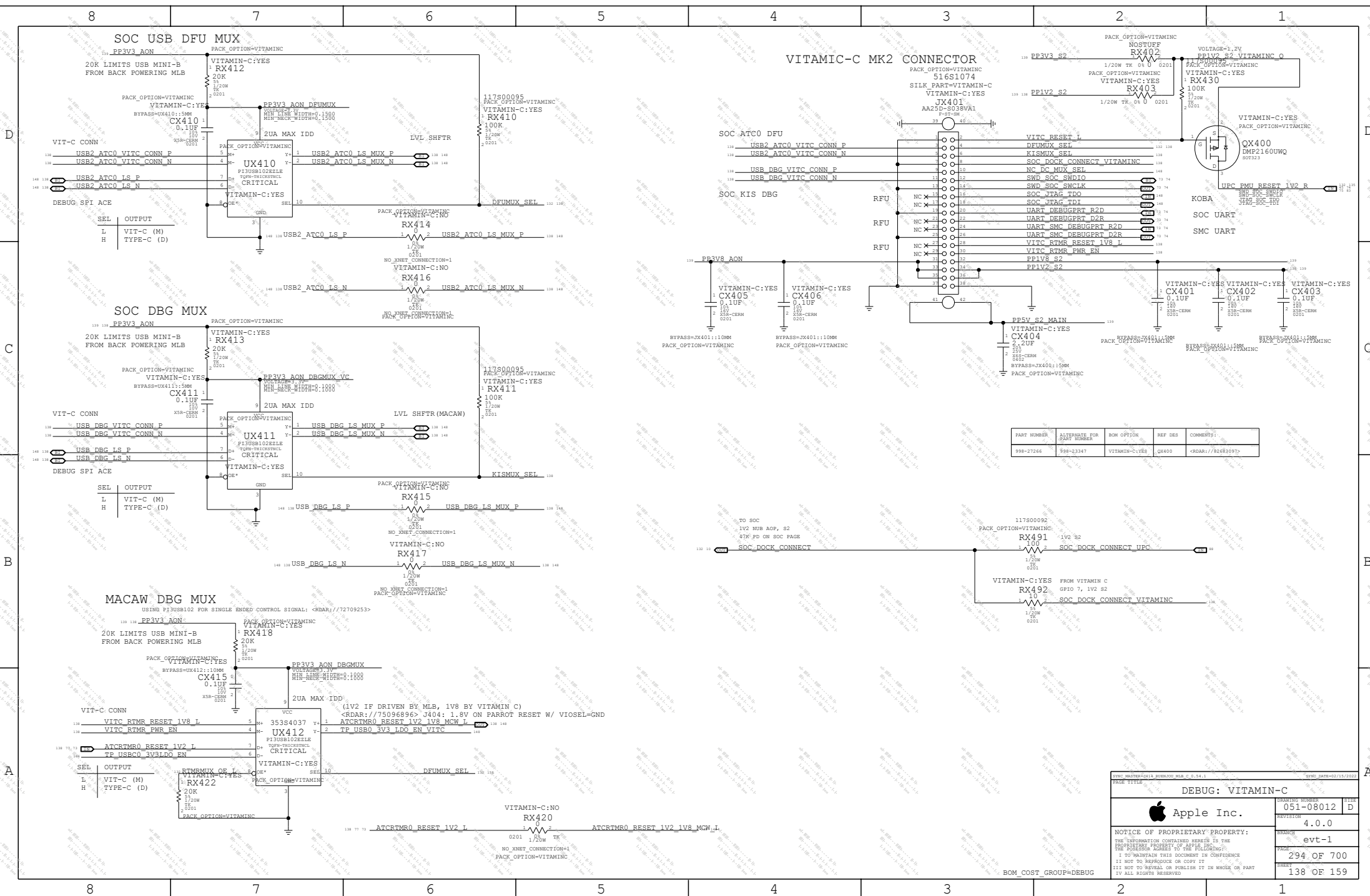
Temp desense caps

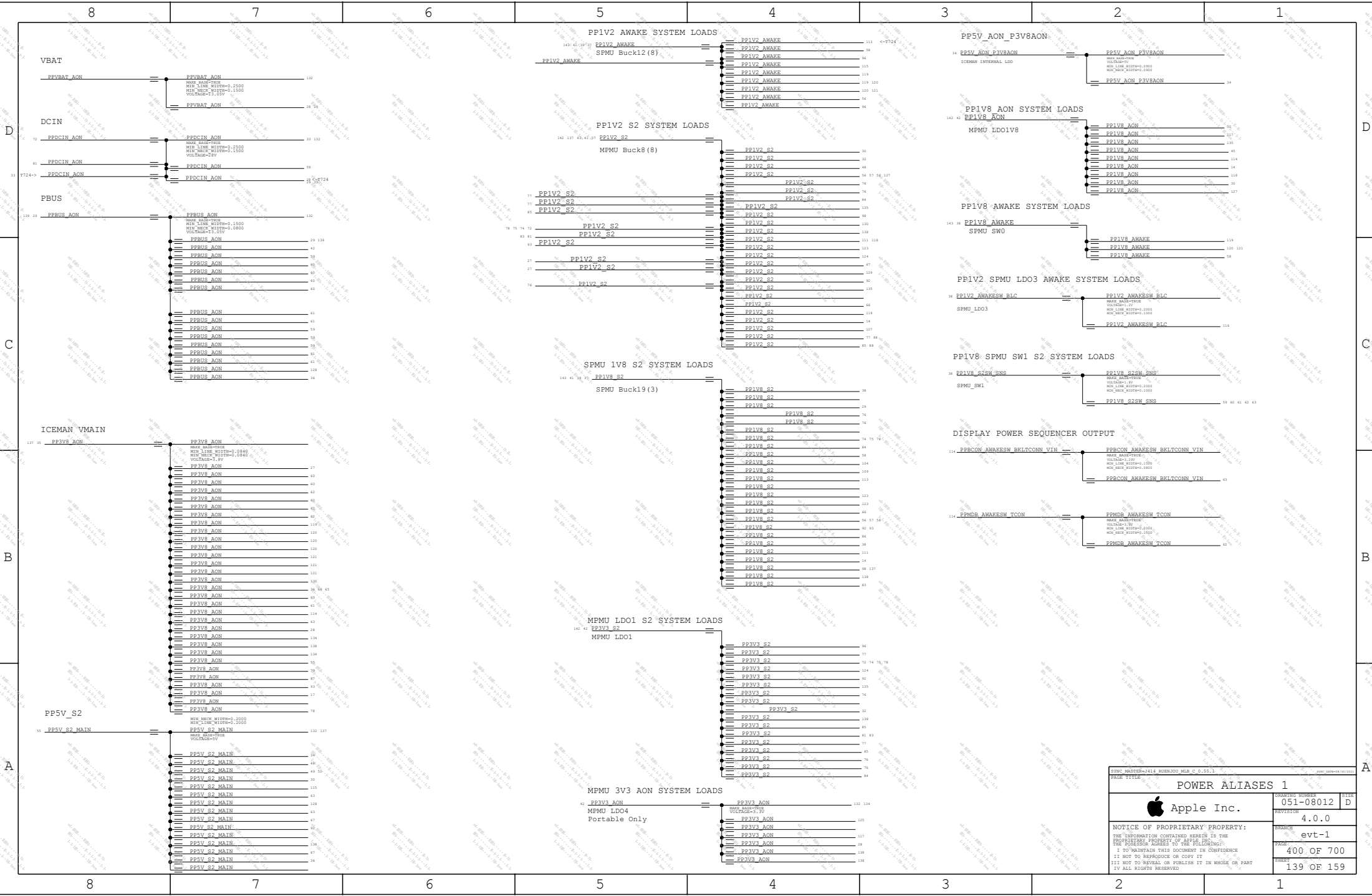


ICEMAN PHASE1 GATE DRIVER desense caps



VDOC: MASTER-0114 81100000 MLC C 0.135.5			
PAGE TITLE			
DESENSE CAPS			
 Apple Inc.	REVISION	051-08012	PAGE D
	REVISION	4.0.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.		REVISION	evt-1
		PAGE	281 OF 700
		PAGE	137 OF 159





D

```
IPD: KEYBOARD / TRACKPAD
PP3V3_S2_IPD (LDO) ALIASES
J414 removed
```



D

C

B

A

D

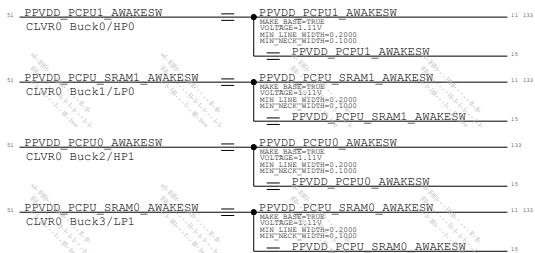
C

B

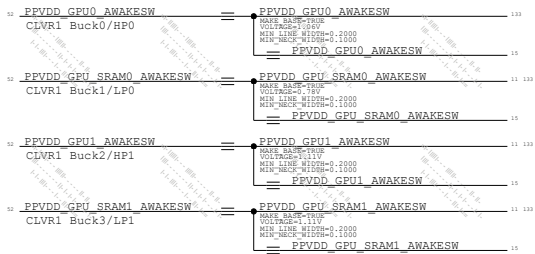
A

CLVR0

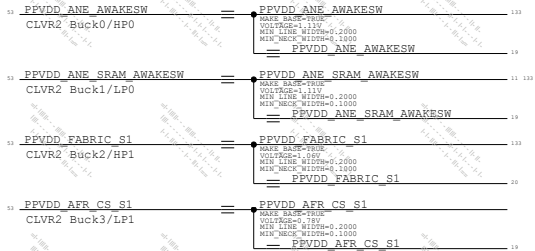
TODO_DT: Update VOLTAGE properties for H14



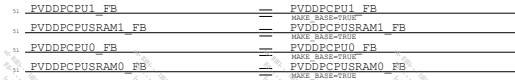
CLVR1



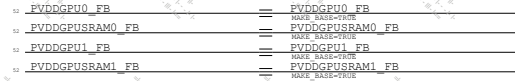
CLVR2



CLVR0



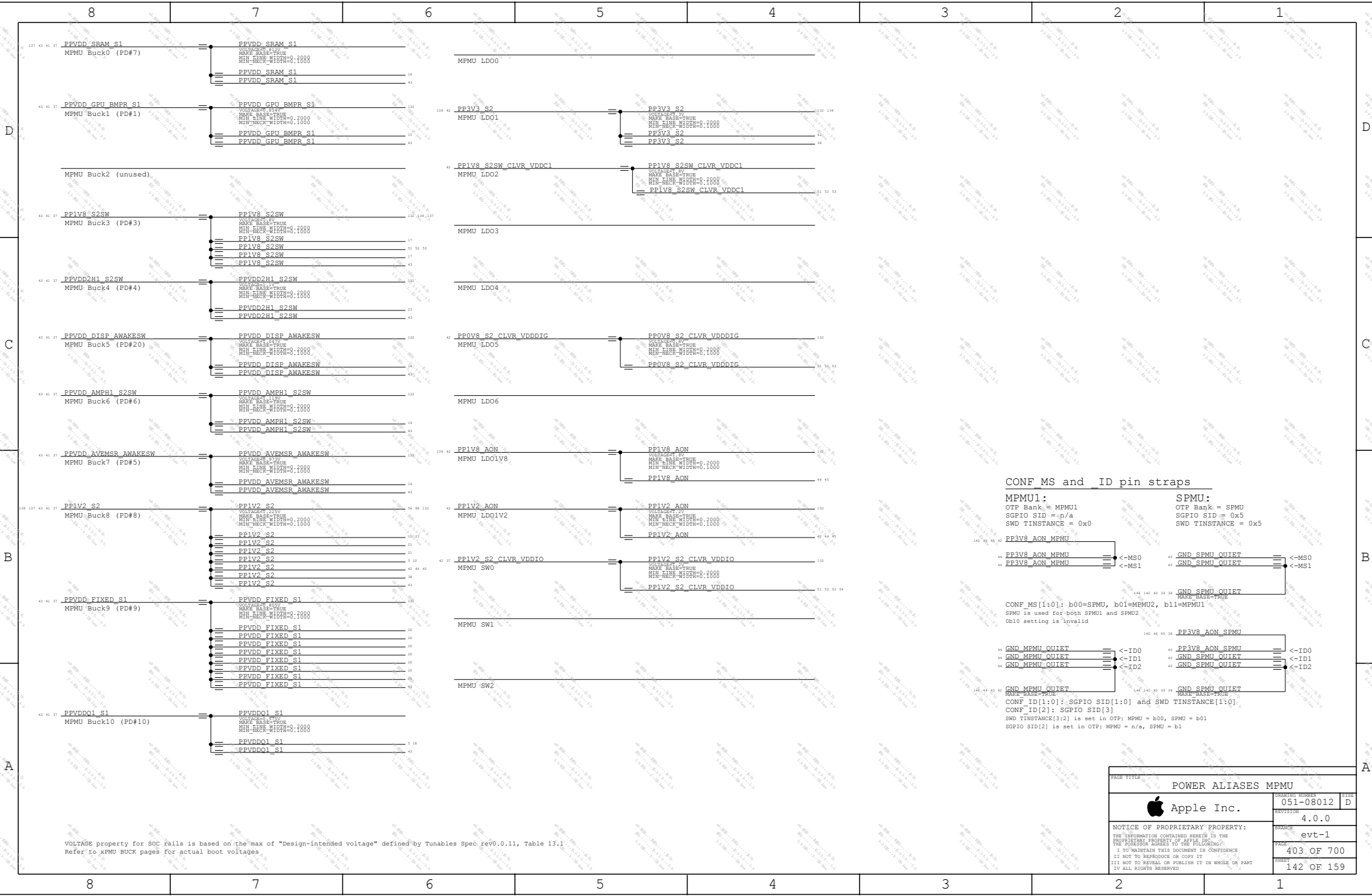
CLVR1



CLVR2



PAGE TITLE			
POWER ALIASES CLVR (S)			
 Apple Inc.	051-08012	DATE	D
	4.0.0	REVISION	
NOTICE OF PROPRIETARY PROPERTY:		ISSUE	evt-1
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN AGREEMENT OF THE FOLLOWING:		PAGE	402 OF 700
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	141 OF 159
IT IS NOT TO BE REPRODUCED OR PUBLISHED IN WHOLE OR PART			
IN ANY MANNER WITHOUT THE WRITTEN AGREEMENT OF APPLE INC.			
ALL RIGHTS RESERVED			



CONF MS and ID pin straps

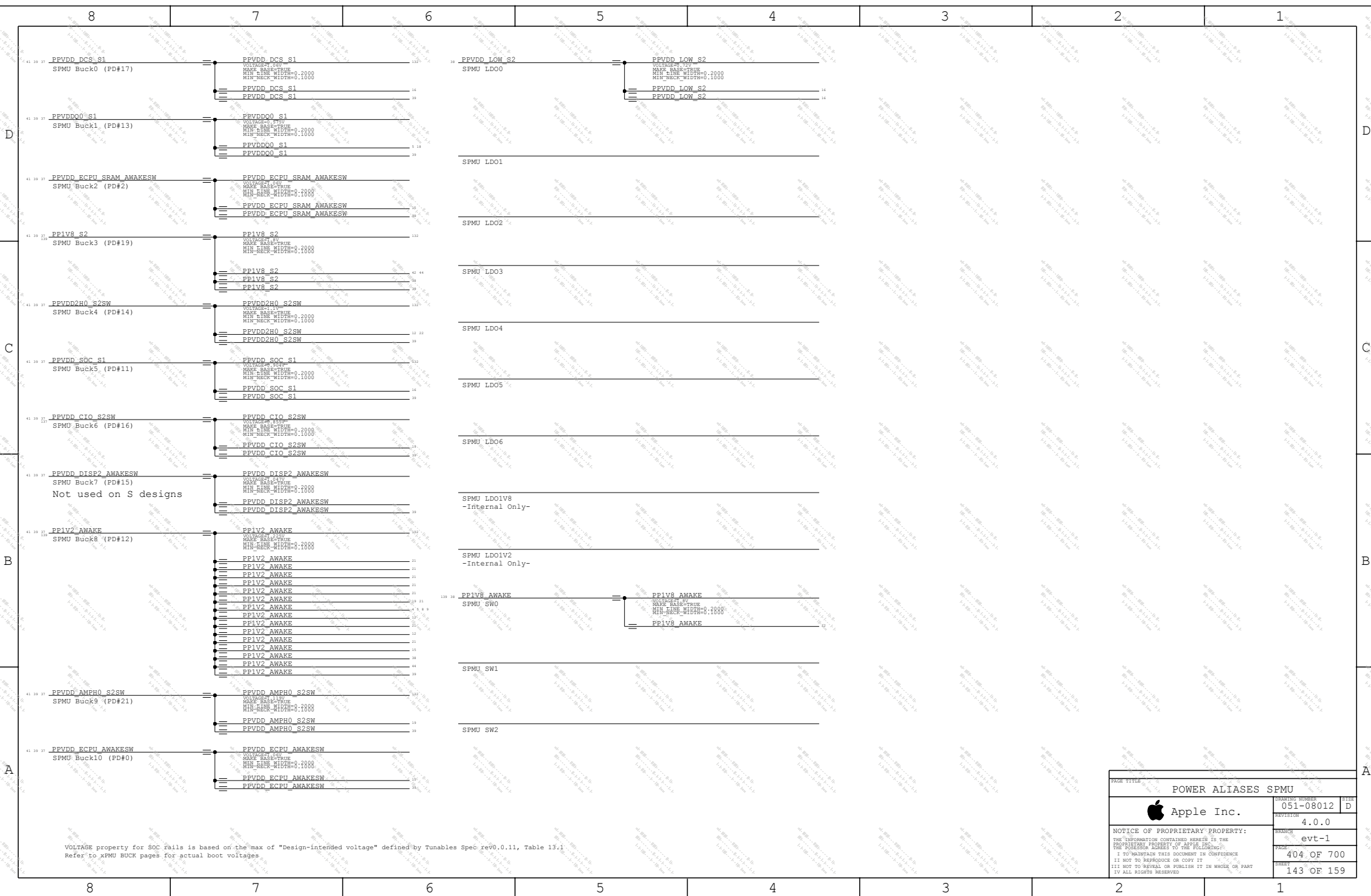
MPMU1:
OTP Bank = MPMU1
SGPIO SID = n/a
SWD TINSTANCE = 0x0

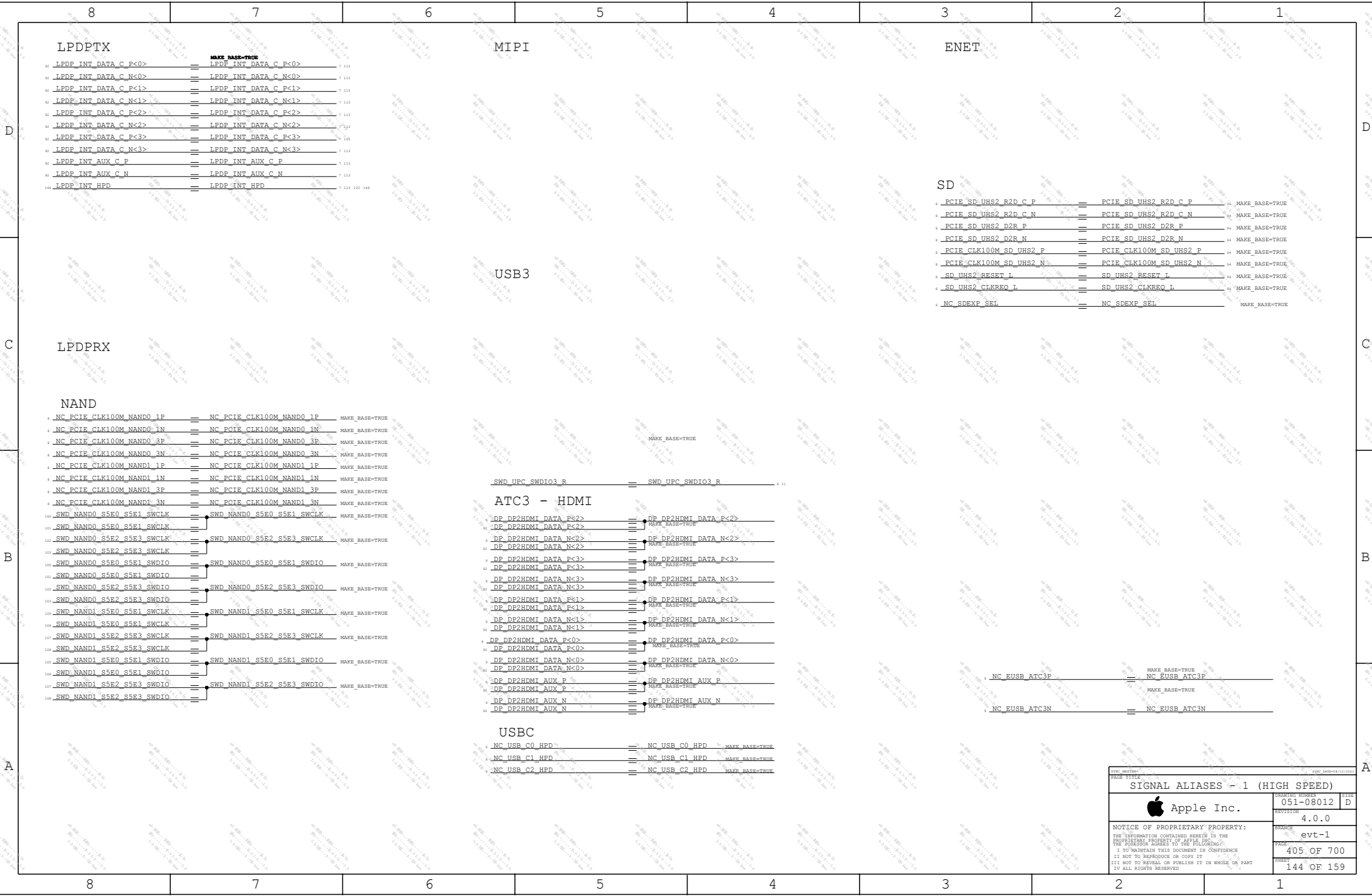
SPMU:
OTP Bank = SPMU
SGPIO SID = 0x5
SWD TINSTANCE = 0x5

CONF MS[1:0]: b00=SPMU, b01=MPMU2, b11=MPMU1
SPMU is used for both SPMU1 and SPMU2
b010 setting is invalid

CONF ID[1:0]: SGPIO SID[1:0] and SWD TINSTANCE[1:0]
CONF ID[2]: SGPIO SID[3]
SWD TINSTANCE[3:2] is set in OTP: MPMU = b00, SPMU = b01
SGPIO SID[2] is set in OTP: MPMU = n/a, SPMU = b1

PAGE TITLE		POWER ALIASES MPMU	
 Apple Inc.	REVISION	051-08012	PAGE D
	REVISION	4.0.0	
NOTICE OF PROPRIETARY PROPERTY:		REVISION	evt-1
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. AND IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE EXPRESS WRITTEN PERMISSION OF APPLE INC.		PAGE	403 OF 700
		SHEET	142 OF 159





Internal signal aliases - Must be configured on project pages per notes below.

Internal signal aliases - Copied or debug circuitry added between.

SOC, series caps

BBR A side

BBR B side

Connector

REMOVED per J414c USBC DRI 003/01/2021

USBC_ATC2_R2D_C_P<1>	==	USBC_ATC2_R2D_C_P<1>	NAVE_BASE-TRUE
USBC_ATC2_R2D_C_NC<1>	==	USBC_ATC2_R2D_C_NC<1>	NAVE_BASE-TRUE
USBC_ATC2_R2D_C_P<2>	==	USBC_ATC2_R2D_C_P<2>	NAVE_BASE-TRUE
USBC_ATC2_R2D_C_NC<2>	==	USBC_ATC2_R2D_C_NC<2>	NAVE_BASE-TRUE
USBC_ATC2_D2R_P<1>	==	USBC_ATC2_D2R_P<1>	NAVE_BASE-TRUE
USBC_ATC2_D2R_NC<1>	==	USBC_ATC2_D2R_NC<1>	NAVE_BASE-TRUE
USBC_ATC2_D2R_P<2>	==	USBC_ATC2_D2R_P<2>	NAVE_BASE-TRUE
USBC_ATC2_D2R_NC<2>	==	USBC_ATC2_D2R_NC<2>	NAVE_BASE-TRUE

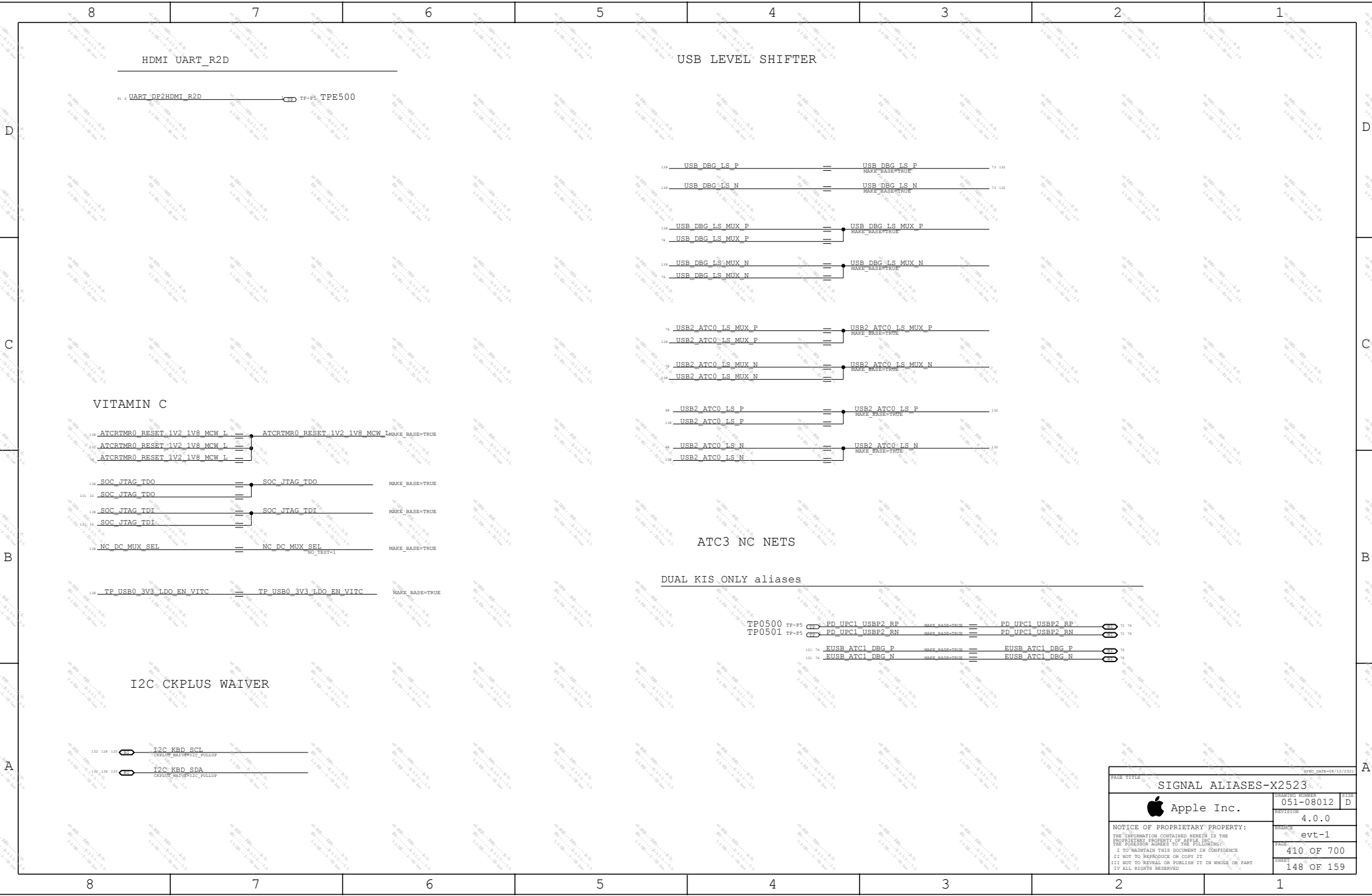
Caps and connector must be aliased to BBR signals.
BBR lanes 1 and 2 can be swapped, both pairs, both sides - all or nothing.
BBR inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

NC_SMC_GPIO6	==	NC_SMC_GPIO6	NAVE_BASE-TRUE
NC_SMC_GPIO7	==	NC_SMC_GPIO7	NAVE_BASE-TRUE
NC_SMC_GPIO8	==	NC_SMC_GPIO8	NAVE_BASE-TRUE
NC_SENSOR0_CLK	==	NC_SENSOR0_CLK	NAVE_BASE-TRUE
NC_NUB_GPIO6	==	NC_NUB_GPIO6	NAVE_BASE-TRUE
NC_NUB_GPIO0	==	NC_NUB_GPIO0	NAVE_BASE-TRUE
NC_LPDPK_RX_D1_P	==	NC_LPDPK_RX_D1_P	NAVE_BASE-TRUE
NC_LPDPK_RX_D1_N	==	NC_LPDPK_RX_D1_N	NAVE_BASE-TRUE
NC_LPDPK_AUX_D0P	==	NC_LPDPK_AUX_D0P	NAVE_BASE-TRUE
NC_LPDPK_AUX_D1P	==	NC_LPDPK_AUX_D1P	NAVE_BASE-TRUE
NC_GP_PCIE_TX2_P	==	NC_GP_PCIE_TX2_P	NAVE_BASE-TRUE
NC_GP_PCIE_TX2_N	==	NC_GP_PCIE_TX2_N	NAVE_BASE-TRUE
NC_GP_PCIE_RX2_P	==	NC_GP_PCIE_RX2_P	NAVE_BASE-TRUE
NC_GP_PCIE_RX2_N	==	NC_GP_PCIE_RX2_N	NAVE_BASE-TRUE
NC_GP_PCIE_REF_CLK2_P	==	NC_GP_PCIE_REF_CLK2_P	NAVE_BASE-TRUE
NC_GP_PCIE_REF_CLK2_N	==	NC_GP_PCIE_REF_CLK2_N	NAVE_BASE-TRUE
NC_GP_PCIE_PERST2_L	==	NC_GP_PCIE_PERST2_L	NAVE_BASE-TRUE
NC_GP_PCIE_CLKREQ2_L	==	NC_GP_PCIE_CLKREQ2_L	NAVE_BASE-TRUE
NC_AP_I2S3_LCKC	==	NC_AP_I2S3_LCKC	NAVE_BASE-TRUE
NC_AP_I2S3_DOUT	==	NC_AP_I2S3_DOUT	NAVE_BASE-TRUE
NC_AP_I2S3_DIN	==	NC_AP_I2S3_DIN	NAVE_BASE-TRUE
NC_AP_I2S3_BCLK	==	NC_AP_I2S3_BCLK	NAVE_BASE-TRUE
NC_AP_GPIO36	==	NC_AP_GPIO36	NAVE_BASE-TRUE
NC_AP_GPIO35	==	NC_AP_GPIO35	NAVE_BASE-TRUE
NC_AOP_UART2_TXD	==	NC_AOP_UART2_TXD	NAVE_BASE-TRUE
NC_AOP_UART2_RXD	==	NC_AOP_UART2_RXD	NAVE_BASE-TRUE

TPT_PAD_MTR_VREFP	==	TPT_PAD_MTR_VREFP	NAVE_BASE-TRUE
TPT_PAD_MTR_VREFN	==	TPT_PAD_MTR_VREFN	NAVE_BASE-TRUE
TPT_PAD_MTR_ANALOG_TESTP	==	TPT_PAD_MTR_ANALOG_TESTP	NAVE_BASE-TRUE
TPT_PAD_MTR_ANALOG_TESTN	==	TPT_PAD_MTR_ANALOG_TESTN	NAVE_BASE-TRUE
TPT_P15VVDNH_DRMOS1_GL1	==	TPT_P15VVDNH_DRMOS1_GL1	NAVE_BASE-TRUE
TPT_P15VVDNH_DRMOS2_GL1	==	TPT_P15VVDNH_DRMOS2_GL1	NAVE_BASE-TRUE
TPT_P15VVDNH_DRMOS3_GL1	==	TPT_P15VVDNH_DRMOS3_GL1	NAVE_BASE-TRUE
TPT_NUB_GPIO8	==	TPT_NUB_GPIO8	NAVE_BASE-TRUE
TPT_MTR_FUNC2	==	TPT_MTR_FUNC2	NAVE_BASE-TRUE
TPT_MTR_FUNC6	==	TPT_MTR_FUNC6	NAVE_BASE-TRUE
TPT_MTR_FUNC7	==	TPT_MTR_FUNC7	NAVE_BASE-TRUE
TPT_COBRA_VDD09_ON	==	TPT_COBRA_VDD09_ON	NAVE_BASE-TRUE
TPT_COBRA_GPIO3	==	TPT_COBRA_GPIO3	NAVE_BASE-TRUE
TPT_COBRA_GPIO2	==	TPT_COBRA_GPIO2	NAVE_BASE-TRUE
TPT_COBRA_GPIO0	==	TPT_COBRA_GPIO0	NAVE_BASE-TRUE
TPT_CHGR_EN_VR1	==	TPT_CHGR_EN_VR1	NAVE_BASE-TRUE
TPT_CHGR_SMC_RST_L	==	TPT_CHGR_SMC_RST_L	NAVE_BASE-TRUE
TPT_CHGR_CBC_ON	==	TPT_CHGR_CBC_ON	NAVE_BASE-TRUE
TPT_BMON_IOUT	==	TPT_BMON_IOUT	NAVE_BASE-TRUE
TPT_ATCRTMR0_TST_CLKOUT	==	TPT_ATCRTMR0_TST_CLKOUT	NAVE_BASE-TRUE
TPT_ATCRTMR1_TST_CLKOUT	==	TPT_ATCRTMR1_TST_CLKOUT	NAVE_BASE-TRUE
TPT_ATCRTMR1_GPIO3	==	TPT_ATCRTMR1_GPIO3	NAVE_BASE-TRUE
TPT_ATCRTMR1_GPIO2	==	TPT_ATCRTMR1_GPIO2	NAVE_BASE-TRUE
TPT_ATCRTMR1_GPIO0	==	TPT_ATCRTMR1_GPIO0	NAVE_BASE-TRUE
TPT_ATCRTMR1_ANALOGMUX_OUT	==	TPT_ATCRTMR1_ANALOGMUX_OUT	NAVE_BASE-TRUE
TPT_ATCRTMR2_TST_CLKOUT	==	TPT_ATCRTMR2_TST_CLKOUT	NAVE_BASE-TRUE
TPT_ATCRTMR2_GPIO3	==	TPT_ATCRTMR2_GPIO3	NAVE_BASE-TRUE
TPT_ATCRTMR2_GPIO2	==	TPT_ATCRTMR2_GPIO2	NAVE_BASE-TRUE
TPT_ATCRTMR2_GPIO0	==	TPT_ATCRTMR2_GPIO0	NAVE_BASE-TRUE
TPT_ATCRTMR2_ANALOGMUX_OUT	==	TPT_ATCRTMR2_ANALOGMUX_OUT	NAVE_BASE-TRUE
TPT_AP_UART2_R2D_RTS_L	==	TPT_AP_UART2_R2D_RTS_L	NAVE_BASE-TRUE
TPT_AP_UART2_R2D	==	TPT_AP_UART2_R2D	NAVE_BASE-TRUE
TPT_AP_UART2_D2R_CTS_L	==	TPT_AP_UART2_D2R_CTS_L	NAVE_BASE-TRUE
TPT_AP_UART2_D2R	==	TPT_AP_UART2_D2R	NAVE_BASE-TRUE
TPT_AP_GPIO39	==	TPT_AP_GPIO39	NAVE_BASE-TRUE
TPT_AP_GPIO38	==	TPT_AP_GPIO38	NAVE_BASE-TRUE
TPT_AP_GPIO37	==	TPT_AP_GPIO37	NAVE_BASE-TRUE
TPT_ANALOGMUX_OUT0	==	TPT_ANALOGMUX_OUT0	NAVE_BASE-TRUE
TPT_ANALOGMUX_OUT1	==	TPT_ANALOGMUX_OUT1	NAVE_BASE-TRUE
TPT_COBRA_GPIO6	==	TPT_COBRA_GPIO6	NAVE_BASE-TRUE

USB2_ATC1_LS_P	==	USB2_ATC1_LS_P	NAVE_BASE-TRUE
USB2_ATC1_LS_N	==	USB2_ATC1_LS_N	NAVE_BASE-TRUE
USB2_ATC2_LS_P	==	USB2_ATC2_LS_P	NAVE_BASE-TRUE
USB2_ATC2_LS_N	==	USB2_ATC2_LS_N	NAVE_BASE-TRUE
EUSB_ATC0_P	==	EUSB_ATC0_P	NAVE_BASE-TRUE
EUSB_ATC0_N	==	EUSB_ATC0_N	NAVE_BASE-TRUE
EUSB_ATC1_P	==	EUSB_ATC1_P	NAVE_BASE-TRUE
EUSB_ATC1_N	==	EUSB_ATC1_N	NAVE_BASE-TRUE
EUSB_ATC2_P	==	EUSB_ATC2_P	NAVE_BASE-TRUE
EUSB_ATC2_N	==	EUSB_ATC2_N	NAVE_BASE-TRUE

8		7		6		5		4		3		2		1	
ISP GPIO				D2D IO				NC SOC							
AOP IO															
SMC GPIO				NC CIO ATC3 LSTX/RX											
ENET GPIO				NC SPN's											
NUB GPIO															
NAND				SOC GPIO TPs BY DOMAIN											
NC SPN's				Nonused SOC pins pulled out by functional/power domains											
ISP SPMI				SOC PP Nets											
AUSTRINGER PWM															
sync from NEW REF SOC H14S															



8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A DIELECTRIC_ONLY	2-10
PLEASE USE HYBRID TABLE	
A DIELECTRIC_ONLY	?

PAGE TITLE		17.2 RULES	
 Apple Inc.		051-08012	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. NO PART OF THIS DOCUMENT IS TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT PERMISSION IN WRITING FROM APPLE INC.		4.0.0	evt-1
		501 OF 700	
		149 OF 159	

[illegible]

SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS		CONSTRAINT SET		COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DOR* DP NAMES EX: DP:DP AA*,DP BB* (LINE STARTS WITH FLAG DP:)	
CLASS NAME					Y/N
I2C	S	A DIELECTRIC 3X			Y
SP1	S	A DIELECTRIC 3X			Y
SPM1	S	A DIELECTRIC 3X			Y
SWD	S	A DIELECTRIC 3X			Y
XTAL	S	A DIELECTRIC 2X			Y
CLOCK 24M	S	A DIELECTRIC 8X			Y
SOC XTAL 24M IN	S	A DIELECTRIC 8X			Y
SOC XTAL 24M OUT	S	A DIELECTRIC 8X			Y
CLOCK 32K	S	A DIELECTRIC 8X			Y
TM LEFT	S	A DIELECTRIC 3X			Y
TM RIGHT	S	A DIELECTRIC 3X			Y
TM CODEC	S	A DIELECTRIC 3X			Y
SPKR IOC	S	A DIELECTRIC 3X			Y
UART	S	A DIELECTRIC 2X			Y
RESETS	S	A DIELECTRIC 3X			Y
WDOG	S	A DIELECTRIC 3X			Y
SOCROT	S	A DIELECTRIC 3X			Y
POWER BUTTON	S	A DIELECTRIC 3X			Y
FAULT	S	A DIELECTRIC 3X			Y
FMIC FDM	S	A DIELECTRIC 3X			Y
FAN CTRL	S	A DIELECTRIC 2X			Y
USBC SOC BSB0 D2R 1	S	A DIELECTRIC 7X			Y
USBC SOC BSB0 D2R 2	S	A DIELECTRIC 7X			Y
USBC SOC BSB0 R2D 1	S	A DIELECTRIC 7X			Y
USBC SOC BSB0 R2D 2	S	A DIELECTRIC 7X			Y
USBC SOC BSB0 AUX	S	A DIELECTRIC 6X			Y
USBC SOC BSB0 L5X	S	A DIELECTRIC 6X			Y
USBC BSB0 CONN D2R 1	S	A DIELECTRIC 7X			Y
USBC BSB0 CONN D2R 2	S	A DIELECTRIC 7X			Y
USBC BSB0 CONN R2D 1	S	A DIELECTRIC 7X			Y
USBC BSB0 CONN R2D 2	S	A DIELECTRIC 7X			Y
USBC BSB0 CONN AUXLSX	S	A DIELECTRIC 6X			Y
USBC UPC0 CONN TOP	S	A DIELECTRIC 5X			Y
USBC UPC0 CONN BOT	S	A DIELECTRIC 5X			Y
USBC UPC0 CONN CC	S	A DIELECTRIC 2X			Y
USBC UPC0 CONN SBU	S	A DIELECTRIC 2X			Y
USBC SOC RMR0 USB2	S	A DIELECTRIC 6X			Y
USBC RMR0 MUX USB2	S	A DIELECTRIC 6X			Y
USBC MIX UPC0 USB2	S	A DIELECTRIC 6X			Y
USBC MIX VTC USB2	S	A DIELECTRIC 6X			Y
USBC SOC BSB1 D2R 1	S	A DIELECTRIC 7X			Y
USBC SOC BSB1 D2R 2	S	A DIELECTRIC 7X			Y
USBC SOC BSB1 R2D 1	S	A DIELECTRIC 7X			Y
USBC SOC BSB1 R2D 2	S	A DIELECTRIC 7X			Y
USBC SOC BSB1 AUX	S	A DIELECTRIC 6X			Y
USBC SOC BSB1 L5X	S	A DIELECTRIC 6X			Y
USBC BSB1 CONN D2R 1	S	A DIELECTRIC 7X			Y
USBC BSB1 CONN D2R 2	S	A DIELECTRIC 7X			Y
USBC BSB1 CONN R2D 1	S	A DIELECTRIC 7X			Y
USBC BSB1 CONN R2D 2	S	A DIELECTRIC 7X			Y
USBC BSB1 CONN AUXLSX	S	A DIELECTRIC 6X			Y
USBC UPC1 CONN TOP	S	A DIELECTRIC 5X			Y
USBC UPC1 CONN BOT	S	A DIELECTRIC 5X			Y
USBC UPC1 CONN CC	S	A DIELECTRIC 2X			Y
USBC UPC1 CONN SBU	S	A DIELECTRIC 2X			Y
USBC SOC RMR1 USB2	S	A DIELECTRIC 6X			Y
USBC RMR1 UPC1 USB2	S	A DIELECTRIC 6X			Y
USBC SOC RMR USB2 DBG	S	A DIELECTRIC 6X			Y
USBC RMR MUX USB2 DBG	S	A DIELECTRIC 6X			Y
USBC MIX UPC USB2 DBG	S	A DIELECTRIC 6X			Y
USBC MIX VTC USB2 DBG	S	A DIELECTRIC 6X			Y
USBC L5X	S	A DIELECTRIC 6X			Y
MIPI FTCAM CLK	S	A DIELECTRIC 6X			Y
MIPI FTCAM DATA	S	A DIELECTRIC 6X			Y
MIPI DFR CLK	S	A DIELECTRIC 6X			Y
MIPI DFR DATA	S	A DIELECTRIC 6X			Y
PCIE WIF1 D2R	S	A DIELECTRIC 7X			Y
PCIE WIF1 R2D	S	A DIELECTRIC 7X			Y
PCIE WIF1 CLK	S	A DIELECTRIC 7X			Y
PCIE NAND0 D2R	S	A DIELECTRIC 7X			Y
PCIE NAND0 R2D	S	A DIELECTRIC 7X			Y
PCIE NAND0 CLK	S	A DIELECTRIC 7X			Y
PCIE NAND1 D2R	S	A DIELECTRIC 7X			Y
PCIE NAND1 R2D	S	A DIELECTRIC 7X			Y
PCIE NAND1 CLK	S	A DIELECTRIC 7X			Y
PCIE CLAREQ	S	A DIELECTRIC 2X			Y
PANEL LEDP DATA	S	A DIELECTRIC 7X			Y
PANEL LEDP AUX	S	A DIELECTRIC 6X			Y
RCAL PCIE	S	A DIELECTRIC 2X			Y
RCAL CIO	S	A DIELECTRIC 2X			Y
RCAL MIPI	S	A DIELECTRIC 2X			Y
RCAL USB	S	A DIELECTRIC 2X			Y
BOARD ID	S	A DIELECTRIC 2X			Y
BOARD REV	S	A DIELECTRIC 2X			Y
WIRELESS TIME SYNC	S	A DIELECTRIC 2X			Y
RBD PWM	S	A DIELECTRIC 2X			Y
GROUND	S	DEFAULT			Y
ANALOG GROUND	S	DEFAULT			Y
AUDIO CONN HEADPHONE OUT	S	A DIELECTRIC 3X			Y
AUDIO CONN RETURN	S	A DIELECTRIC 2X			Y
AUDIO CONN SENSE	S	A DIELECTRIC 2X			Y
SPEAKERAMP OUTPUT	S	A DIELECTRIC 2X			Y
SENSE DIVP	S	A DIELECTRIC 2X			Y
RF ANTENNA	S	DEFAULT			Y
RFO BUCK FB	S	DEFAULT			Y
POWER	S	DEFAULT			Y

CLASS DEFINITIONS		CONSTRAINT SET		COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DOR* DP NAMES EX: DP:DP AA*,DP BB* (LINE STARTS WITH FLAG DP:)	
CLASS NAME					Y/N
USBC SOC BSB2 D2R 1	S	A DIELECTRIC 7X			Y
USBC SOC BSB2 D2R 2	S	A DIELECTRIC 7X			Y
USBC SOC BSB2 R2D 1	S	A DIELECTRIC 7X			Y
USBC SOC BSB2 R2D 2	S	A DIELECTRIC 7X			Y
USBC SOC BSB2 AUX	S	A DIELECTRIC 6X			Y
USBC SOC BSB2 L5X	S	A DIELECTRIC 6X			Y
USBC BSB2 CONN D2R 1	S	A DIELECTRIC 7X			Y
USBC BSB2 CONN D2R 2	S	A DIELECTRIC 7X			Y
USBC BSB2 CONN R2D 1	S	A DIELECTRIC 7X			Y
USBC BSB2 CONN R2D 2	S	A DIELECTRIC 7X			Y
USBC BSB2 CONN AUXLSX	S	A DIELECTRIC 6X			Y
USBC UPC2 CONN TOP	S	A DIELECTRIC 5X			Y
USBC UPC2 CONN BOT	S	A DIELECTRIC 5X			Y
USBC UPC2 CONN CC	S	A DIELECTRIC 2X			Y
USBC UPC2 CONN SBU	S	A DIELECTRIC 2X			Y
USBC SOC RMR2 USB2	S	A DIELECTRIC 6X			Y
USBC RMR2 MUX USB2	S	A DIELECTRIC 6X			Y
USBC MIX UPC2 USB2	S	A DIELECTRIC 6X			Y
HDMI CLK CONN	S	A DIELECTRIC 6X			Y
HDMI MADEA CONN DATA	S	A DIELECTRIC 6X			Y
SOC MADEA DATA	S	A DIELECTRIC 6X			Y
SW NODE	S	A DIELECTRIC 6X			Y

8

7

6

5

4

3

2

1

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	GROUND	DEFAULT
SP1	GROUND	DEFAULT
SPM1	GROUND	DEFAULT
SWD	GROUND	DEFAULT
JTAG	GROUND	DEFAULT
CLOCK 24M	GROUND	DEFAULT
CLOCK 32K	GROUND	DEFAULT
TM LEFT	GROUND	DEFAULT
TM RIGHT	GROUND	DEFAULT
TM CODEC	GROUND	DEFAULT
SPKR IOC	GROUND	DEFAULT
UART	GROUND	DEFAULT
RESETS	GROUND	DEFAULT
WDOG	GROUND	DEFAULT
SOCBOT	GROUND	DEFAULT
POWER BUTTON	GROUND	DEFAULT
FAULT	GROUND	DEFAULT
DMIC PWM	GROUND	DEFAULT
FAN CTRL	GROUND	DEFAULT
USBC SOC BSB0 D2R 1	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB0 D2R 2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB0 R2D 1	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB0 R2D 2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB0 AUX	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB0 LSX	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC BSB0 CONN D2R 1	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC BSB0 CONN D2R 2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC BSB0 CONN R2D 1	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC BSB0 CONN R2D 2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC BSB0 CONN AUXLSX	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC UPC0 CONN TOP	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC UPC0 CONN BOT	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC UPC0 CONN CC	GROUND	DEFAULT
USBC UPC0 CONN SBU	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC RTMR0 USB2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC RTMR0 MUX USB2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC MUX UPC0 USB2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC MUX VITC USB2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 D2R 1	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 D2R 2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 R2D 1	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 R2D 2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 AUX	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 LSX	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC BSB1 CONN D2R 1	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC BSB1 CONN D2R 2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC BSB1 CONN R2D 1	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC BSB1 CONN R2D 2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC BSB1 CONN AUXLSX	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC UPC1 CONN TOP	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC UPC1 CONN BOT	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC UPC1 CONN CC	GROUND	DEFAULT
USBC UPC1 CONN SBU	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC RTMR1 USB2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC RTMR1 UPC1 USB2	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC SOC RTMR USB2 DBG	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC RTMR MUX USB2 DBG	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC MUX UPC USB2 DBG	GROUND	DEFAULT WITH 5X LINE2SHAPE
USBC MUX VITC USB2 DBG	GROUND	DEFAULT WITH 5X LINE2SHAPE
MIPI FTCAM CLK	GROUND	DEFAULT WITH 5X LINE2SHAPE
MIPI FTCAM DATA	GROUND	DEFAULT WITH 5X LINE2SHAPE
MIPI DPM CLK	GROUND	DEFAULT WITH 5X LINE2SHAPE
MIPI DPM DATA	GROUND	DEFAULT WITH 5X LINE2SHAPE
PCIE WIFI D2R	GROUND	DEFAULT WITH 5X LINE2SHAPE
PCIE WIFI R2D	GROUND	DEFAULT WITH 5X LINE2SHAPE
PCIE WIFI CLK	GROUND	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND0 D2R	GROUND	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND0 R2D	GROUND	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND0 CLK	GROUND	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND1 D2R	GROUND	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND1 R2D	GROUND	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND1 CLK	GROUND	DEFAULT WITH 5X LINE2SHAPE
PCIE CLASBQ	GROUND	DEFAULT
PANEL LPDP DATA	GROUND	DEFAULT WITH 5X LINE2SHAPE
PANEL LPDP AUX	GROUND	DEFAULT WITH 5X LINE2SHAPE
RCAL PCIE	GROUND	DEFAULT
RCAL CIO	GROUND	DEFAULT
RCAL MIPI	GROUND	DEFAULT
BOARD ID	GROUND	DEFAULT
BOARD REV	GROUND	DEFAULT
WIRELESS TIME SYNC	GROUND	DEFAULT
KBD PWM	GROUND	DEFAULT
AUDIO CONN HEADPHONE OUT	GROUND	DEFAULT
AUDIO CONN RETURN	GROUND	DEFAULT
AUDIO CONN SENSE	GROUND	DEFAULT
SPEAKERAMP OUTPUT	GROUND	DEFAULT
SENSE DIFF	GROUND	DEFAULT
SOC XTAL 24M IN	GROUND	DEFAULT
SOC XTAL 24M OUT	GROUND	DEFAULT
POWER	GROUND	DEFAULT

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	POWER	DEFAULT
SP1	POWER	DEFAULT
SPM1	POWER	DEFAULT
SWD	POWER	DEFAULT
JTAG	POWER	DEFAULT
CLOCK 24M	POWER	DEFAULT
CLOCK 32K	POWER	DEFAULT
TM LEFT	POWER	DEFAULT
TM RIGHT	POWER	DEFAULT
TM CODEC	POWER	DEFAULT
SPKR IOC	POWER	DEFAULT
UART	POWER	DEFAULT
RESETS	POWER	DEFAULT
WDOG	POWER	DEFAULT
SOCBOT	POWER	DEFAULT
POWER BUTTON	POWER	DEFAULT
FAULT	POWER	DEFAULT
DMIC PWM	POWER	DEFAULT
FAN CTRL	POWER	DEFAULT
USBC SOC BSB0 D2R 1	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB0 D2R 2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB0 R2D 1	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB0 R2D 2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB0 AUX	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB0 LSX	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC BSB0 CONN D2R 1	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC BSB0 CONN D2R 2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC BSB0 CONN R2D 1	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC BSB0 CONN R2D 2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC BSB0 CONN AUXLSX	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC UPC0 CONN TOP	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC UPC0 CONN BOT	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC UPC0 CONN CC	POWER	DEFAULT
USBC UPC0 CONN SBU	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC RTMR0 USB2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC RTMR0 MUX USB2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC MUX UPC0 USB2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC MUX VITC USB2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 D2R 1	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 D2R 2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 R2D 1	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 R2D 2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 AUX	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC BSB1 LSX	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC BSB1 CONN D2R 1	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC BSB1 CONN D2R 2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC BSB1 CONN R2D 1	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC BSB1 CONN R2D 2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC BSB1 CONN AUXLSX	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC UPC1 CONN TOP	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC UPC1 CONN BOT	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC UPC1 CONN CC	POWER	DEFAULT
USBC UPC1 CONN SBU	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC RTMR1 USB2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC RTMR1 UPC1 USB2	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC SOC RTMR USB2 DBG	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC RTMR MUX USB2 DBG	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC MUX UPC USB2 DBG	POWER	DEFAULT WITH 5X LINE2SHAPE
USBC MUX VITC USB2 DBG	POWER	DEFAULT WITH 5X LINE2SHAPE
MIPI FTCAM CLK	POWER	DEFAULT WITH 5X LINE2SHAPE
MIPI FTCAM DATA	POWER	DEFAULT WITH 5X LINE2SHAPE
MIPI DPM CLK	POWER	DEFAULT WITH 5X LINE2SHAPE
MIPI DPM DATA	POWER	DEFAULT WITH 5X LINE2SHAPE
PCIE WIFI D2R	POWER	DEFAULT WITH 5X LINE2SHAPE
PCIE WIFI R2D	POWER	DEFAULT WITH 5X LINE2SHAPE
PCIE WIFI CLK	POWER	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND0 D2R	POWER	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND0 R2D	POWER	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND0 CLK	POWER	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND1 D2R	POWER	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND1 R2D	POWER	DEFAULT WITH 5X LINE2SHAPE
PCIE NAND1 CLK	POWER	DEFAULT WITH 5X LINE2SHAPE
PCIE CLASBQ	POWER	DEFAULT
PANEL LPDP DATA	POWER	DEFAULT WITH 5X LINE2SHAPE
PANEL LPDP AUX	POWER	DEFAULT WITH 5X LINE2SHAPE
RCAL PCIE	POWER	DEFAULT
RCAL CIO	POWER	DEFAULT
RCAL MIPI	POWER	DEFAULT
BOARD ID	POWER	DEFAULT
BOARD REV	POWER	DEFAULT
WIRELESS TIME SYNC	POWER	DEFAULT
KBD PWM	POWER	DEFAULT
AUDIO CONN HEADPHONE OUT	POWER	DEFAULT
AUDIO CONN RETURN	POWER	DEFAULT
AUDIO CONN SENSE	POWER	DEFAULT
SPEAKERAMP OUTPUT	POWER	DEFAULT
SENSE DIFF	POWER	DEFAULT
SOC XTAL 24M IN	POWER	DEFAULT
SOC XTAL 24M OUT	POWER	DEFAULT
POWER	POWER	DEFAULT

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
USBC SOC BSB0 D2R 1	USBC SOC BSB0 D2R 2	A DIELECTRIC 5X
USBC SOC BSB0 R2D 1	USBC SOC BSB0 R2D 2	A DIELECTRIC 5X
USBC BSB0 CONN D2R 1	USBC BSB0 CONN D2R 2	A DIELECTRIC 5X
USBC BSB0 CONN R2D 1	USBC BSB0 CONN R2D 2	A DIELECTRIC 5X
USBC SOC BSB1 D2R 1	USBC SOC BSB1 D2R 2	A DIELECTRIC 5X
USBC SOC BSB1 R2D 1	USBC SOC BSB1 R2D 2	A DIELECTRIC 5X
USBC BSB1 CONN D2R 1	USBC BSB1 CONN D2R 2	A DIELECTRIC 5X
USBC BSB1 CONN R2D 1	USBC BSB1 CONN R2D 2	A DIELECTRIC 5X
PANEL LPDP DATA	PANEL LPDP DATA	A DIELECTRIC 5X
SOC XTAL 24M IN	SOC XTAL 24M OUT	A DIELECTRIC 2X

8

7

6

5

4

3

2

1

7.2 SPACING CSETS, CLASS-CLASS	
Apple Inc.	051-08012
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. IT IS TO BE KEPT CONFIDENTIAL AND NOT TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE EXPRESS WRITTEN PERMISSION OF APPLE INC.	4.0.0
504 OF 700	152 OF 159

USBC page BOM
Multi-protocol Retimer(Lifuka)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-21959	3	IC,RTMR,AL,USB-C RETIMER,FC05154	UF000,UF100,UG000	CRITICAL	RT13:AO
338800773	3	IC,LFPR,AL,USB-C RETIMER,C05154	UF000,UF100,UG000	CRITICAL	RT13:BO_MP
998-00304	3	IC,RTMR,AL,USB-C RETIMER,DEV,C05154	UF000,UF100,UG000	CRITICAL	RT13:BO
998-27476	3	IC,LFPR,AL,USB-C RETIMER,DEV,C05154	UF000,UF100,UG000	CRITICAL	RT13:BI_DEV
338800889	3	IC,LFPR,AL,USB-C RETIMER,ATX,C05154	UF000,UF100,UG000	CRITICAL	RT13:BI_ATX_PROD
338800889	3	IC,LFPR,AL,USB-C RETIMER,RCX,C05154	UF000,UF100,UG000	CRITICAL	RT13:BI_RCX_PROD
338800890	3	IC,LFPR,AL,USB-C RETIMER,ASE,C05154	UF000,UF100,UG000	CRITICAL	RT13:BI_ASE_PROD
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
338800889	338800888			REPLACES PART	
338800890	338800888			REPLACES PART	

Ace2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338802742	3	IC,USBA,AL,USB 2.0 HUB,80400000	US000,UF000,UG000	CRITICAL	USBCPC:R0M2
338802993	3	IC,USBA,AL,USB 2.0 HUB,80400000	US000,UF000,UG000	CRITICAL	USBCPC:R0M3

USB level shifter-MACAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338800914	3	IC,MACAM,CY000400,AL,C05154	UF000,UF000,UG000	CRITICAL	MACAM:A2
998-20194	3	IC,MACAM,CY000400,AL,C05154	UF000,UF000,UG000	CRITICAL	MACAM:A1
998-26776	3	IC,MACAM,CY000400,AL,C05154	UF000,UF000,UG000	CRITICAL	MACAM:IOA02_1

Re-timer Sequencer

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343800030	2	IC,USBA,AL,USB 2.0 HUB,80400000	UF000,UF000,UG000	CRITICAL	

Re-timer ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335800574	3	IC,FLASH,64MBIT,1.2V,QS-1,W,4X4MM,ROM8	UF090,UF190,UG090	CRITICAL	ATCRTHR_ROM:WINBOND
335800575	3	IC,FLASH,64MBIT,1.2V,QS-1,W,4X4MM,ROM8	UF090,UF190,UG090	CRITICAL	ATCRTHR_ROM:MACRONIX
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
335800575	335800574			CRITICAL	

Programmable parts: ACE ROMs (CURRENT in BOM)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341802110	1	ROM,ACE-P01 (V3.011.0.4) P1A-R3,K2371	UF250	CRITICAL	ACE_ROM:V3_011
341802110	1	ROM,ACE-P01 (V3.011.0.4) P1B-R3,K2371	UF260	CRITICAL	ACE_ROM:V3_011
341802111	1	ROM,ACE-P2 (V3.011.0.4) P1B-R3,K2371	UG260	CRITICAL	ACE_ROM:V3_011
341802112	1	ROM,ACE-P5 (V3.011.0.4) P1B-R3,K2371	U5560	CRITICAL	ACE_ROM:V3_011
335800133	1	ROM,K2371	UF250,UF260,UG260,U5560	CRITICAL	ACE_ROM:BLANK

ACE BOM BLANK ALT parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
335800337	335800133	ACE_ROM:BLANK			
335800571	335800133	ACE_ROM:BLANK			

335800570 is removed per radar 82361417

Programmable parts: ACE ROMs- PREVIOUS BUILDS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341802056	1	ROM,ACE-P01 (V3.006.0.4) P1A-R3,K2371	UF250	CRITICAL	ACE_ROM:PIA-R3
341802056	1	ROM,ACE-P01 (V3.006.0.4) P1A-R3,K2371	UF260	CRITICAL	ACE_ROM:PIA-R3
341802057	1	ROM,ACE-P2 (V3.006.0.4) P1A-R3,K2371	UG260	CRITICAL	ACE_ROM:PIA-R3
341802058	1	ROM,ACE-P5 (V3.006.0.4) P1A-R3,K2371	U5560	CRITICAL	ACE_ROM:PIA-R3

NAND PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335800559	1	NAND,HCST,192GB,68E,XX,X,512G,W,UGA315	UN000	CRITICAL	NAND:TS-512
335800551	3	NAND,HCST,128GB,68E,XX,X,512G,W,UGA315	UN100,UN200,UN300	CRITICAL	NAND:TS-512
335800565	1	NAND,HCST,192GB,68E,XX,X,512G,W,UGA315	UN000	CRITICAL	NAND:WD-512
335800548	3	NAND,HCST,128GB,68E,XX,X,512G,W,UGA315	UN100,UN200,UN300	CRITICAL	NAND:WD-512
335800579	4	NAND,HCST,128GB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-512
335800552	4	NAND,HCST,256GB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-1TB
335800581	4	NAND,HCST,256GB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-1TB
335800549	4	NAND,HCST,256GB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-1TB
335800553	4	NAND,HCST,512GB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-2TB
335800583	4	NAND,HCST,512GB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:HY-2TB
335800550	4	NAND,HCST,512GB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-2TB
335800553	4	NAND,HCST,512GB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-4TB
335800553	4	NAND,HCST,512GB,68E,XX,X,512G,W,UGA315	UN000,UN600,UN700,UN800	CRITICAL	NAND:TS-4TB
335800550	4	NAND,HCST,512GB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-4TB
335800550	4	NAND,HCST,512GB,68E,XX,X,512G,W,UGA315	UN000,UN600,UN700,UN800	CRITICAL	NAND:WD-4TB
335800561	4	NAND,HCST,1TB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:TS-8TB
335800561	4	NAND,HCST,1TB,68E,XX,X,512G,W,UGA315	UN000,UN600,UN700,UN800	CRITICAL	NAND:TS-8TB
335800567	4	NAND,HCST,1024GB,68E,XX,X,512G,W,UGA315	UN000,UN100,UN200,UN300	CRITICAL	NAND:WD-8TB
335800567	4	NAND,HCST,1024GB,68E,XX,X,512G,W,UGA315	UN000,UN600,UN700,UN800	CRITICAL	NAND:WD-8TB
335800552	2	NAND,HCST,256GB,68E,XX,X,512G,W,UGA315	UN000,UN100	CRITICAL	NAND:K2L-512
335800581	2	NAND,HCST,256GB,68E,XX,X,512G,W,UGA315	UN000,UN100	CRITICAL	NAND:W2L-512
335800549	2	NAND,HCST,256GB,68E,XX,X,512G,W,UGA315	UN000,UN100	CRITICAL	NAND:W2L-512

NAND SOCKET

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-11766	2	PCBA,NAND,K2371	UN000,UN600	CRITICAL	NAND:SOCKET

10/08/2021	
USBC & NAND BOM OPTION	
 Apple Inc.	051-08012
	4.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. IT IS NOT TO BE REPRODUCED OR COPIED IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.	evt-1
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE AND NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE INC.	600 OF 700
	153 OF 159

SOC-DEV/SOCKET

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-16917	1	SOC, SOC, DEV	U0600	CRITICAL	SOC:DEV
939-12686	1	PCB, HONG KONG, K2371	U0600	CRITICAL	SOC:SOCKET

NOTE 05/27/2022

Per email from Simon
BIN1, BIN2, BIN5 in the excel sheetPer email from Mikio 05/25/2022
BIN1, BIN5 are J414s POR

SOC-A1-J414s EVTS BUILD 05/27/22

Bin1 = 8C,19FSTP

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-29172	1	SOC, RMD-S A1+32G, 1V, 8C, BIN1, LP, AG, H, R3103	U0600	CRITICAL	SOC:8C_19FSTP_32G
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-29174	998-29172	ANY	ALL	RM-S-A1 32G LP BIN1 ALT-MICRO	
998-29176	998-29172	ANY	ALL	RM-S-A1 32G BIN2 ALT-HY	
998-29178	998-29172	ANY	ALL	RM-S-A1 32G BIN2 ALT-MICRO	

IFP, LP

Bin1 = 8C,19FSTP
BIN2 is ALT to Bin1

32G HYNIX

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-29171	1	SOC, RMD-S A1+16G, 1V, 8C, BIN1, LP, AG, H, R3103	U0600	CRITICAL	SOC:8C_19FSTP_16G
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-29173	998-29171	ANY	ALL	RM-S-A1 16G LP BIN1 ALT-MICRO	
998-29175	998-29171	ANY	ALL	RM-S-A1 16G BIN2 ALT-HY	
998-29177	998-29171	ANY	ALL	RM-S-A1 16G BIN2 ALT-MICRO	

IFP, LP

Bin1 = 8C,19FSTP
BIN2 is ALT to Bin1

16G HYNIX

Bin5 = 6C,16FSTP new APN for EVTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-29184	1	SOC, RMD-S A1+32G, 1V, 6C, BIN5, AG, H, R3103	U0600	CRITICAL	SOC:6C_16FSTP_32G
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-29186	998-29184	ANY	ALL	A1 32G BINS ALT-MICRO	

Bin5 = 6C,16FSTP

32G HYNIX

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-29183	1	SOC, RMD-S A1+16G, 1V, 6C, BIN5, AG, H, R3103	U0600	CRITICAL	SOC:6C_16FSTP_16G
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-29185	998-29183	ANY	ALL	A1 16G BINS ALT-MICRO	

Bin5 = 6C,16FSTP

16G HYNIX

Bin3 = 8C,16FSTP

Bin3 REMOVED for EVTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-28138	1	SOC, RMD-S A1+32G, 1V, 8C, BIN3, AG, H, R3103	U0600	CRITICAL	SOC:8C_16FSTP_32G
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-28140	998-28138	ANY	ALL	A0 32G 16FSTP BIN3 ALT-MICRO	
998-28347	998-28138	ANY	ALL	A0 32G 19FSTP LP BIN1 ALT-HY	
998-28349	998-28138	ANY	ALL	A0 32G 19FSTP LP BIN1 ALT-MICRO	

Bin3 = 8C,16FSTP

32G HYNIX

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-28137	1	SOC, RMD-S A1+16G, 1V, 8C, BIN3, AG, H, R3103	U0600	CRITICAL	SOC:8C_16FSTP_16G
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-28139	998-28137	ANY	ALL	A0 16G 16FSTP BIN3 ALT-MICRO	
998-28566	998-28137	ANY	ALL	A0 16G 19FSTP LP BIN1 ALT-HY	
998-28568	998-28137	ANY	ALL	A0 16G 19FSTP LP BIN1 ALT-MICRO	

Bin3 = 8C,16FSTP

16G HYNIX

EOS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00814	1	IC, EOS SM300V, B0, DEV, 780, WLCS979	U5000	CRITICAL	EOS:DEV
338S00877	1	IC, EOS SM300V, B1, DEV, 780, WLCS979	U5000	CRITICAL	EOS:B1_DEV

HDMI COBRA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-25553	1	IC, COBRA, A0, DP TO HDMI CONVTR, DEV, B0A120	UH700	CRITICAL	COBRA:CFG1
338S00772	1	IC, COBRA, A0, PS190, DP TO HDMI, A0, B0A120	UH700	CRITICAL	COBRA:CFG2

HDMI SAK

in CSA178

HMDI CONNECTOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514S00360	1	CONN, RCPT, BLK, HDMI, X1982	JH500	CRITICAL	

BLACK

OCARINA 0/1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00600	1	IC, PMU, OCARINA, D2499A0, OPT-BC, WLCS956	UN400	CRITICAL	OCARINA:A0_OTPBC
338S00600	1	IC, PMU, OCARINA, D2499A0, OPT-BC, WLCS956	UN900	CRITICAL	OCARINA:A0_OTPBC

SD CARD CONNECTOR BOM OPTIONS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-00196	1	CONN, RCPT, BLK, SD, X1982	JK600	CRITICAL	

BLACK

WHAMOLA APN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S02937	1	IC, RAA689900, PMIC, WHAMOLA, OTP-S, WCEP40	U5200	CRITICAL	WHAMOLA:LA416
353S02781	1	IC, RAA689900, PMIC, WHAMOLA, OTP-S, WCEP40	U5200	CRITICAL	WHAMOLA:OA936

PBUS CAPS not call C5210

BOM OPTION TABLES-2		DATE
Apple Inc.		D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF APPLE INC. IT IS TO BE KEPT CONFIDENTIAL AND NOT TO BE REPRODUCED OR DISCLOSED TO ANY OTHER PARTY WITHOUT THE WRITTEN PERMISSION OF APPLE INC.		REV
601 OF 700		REV
154 OF 159		REV

	8	7	6	5	4	3	2	1																																																																														
D	COMMON BOM GROUPS				BOM Variants																																																																																	
	<table><tr><th>BOM GROUP</th><th colspan="3">BOM OPTIONS</th></tr><tr><td>X2523_COMMON</td><td colspan="3">SCH,PCB,COMMON,ALT_CM,ALTERNATE:INSTANCE,X2523_COMMON1,X2523_COMMON2,X2523_PROGPARTS,X2523_BLC,X2523_BOS,X2523_HDMI,X2523_SOC,X2523_USBC,X2523_FWR</td></tr><tr><td>X2523_COMMON1</td><td colspan="3">BOARD_ID,BOARD_REV:0011,BOOTCFG2</td></tr><tr><td>X2523_COMMON2</td><td colspan="3">RF_CONN,REFIDU_IC:HMI286,BTFNR,VITAMIN-C:NG</td></tr><tr><td>X2523_PROGPARTS</td><td colspan="3">ATCCTR_BOM:WINBOND,ACE_ROM:V3_011,HDMI_ROM:FREEP</td></tr><tr><td>X2523_BLC</td><td colspan="3">BLC_BEN_IC:V4,BLC_SV_SERIES:I10_OHM,BLC_SV_CAP:4P7_UF</td></tr><tr><td>X2523_BOS</td><td colspan="3">BOS:B1_DEV</td></tr><tr><td>X2523_HDMI</td><td colspan="3">CONRA:CFG2,CONRAPART:0,DATA_FILT,HDMI_CLC_FILT:YES,LDO_HDMI:SV</td></tr><tr><td>X2523_SOC</td><td colspan="3">DRAMST:PMIO,VDDIEM:1777</td></tr><tr><td>X2523_USBC</td><td colspan="3">ACE_WILL_BE_OTFED:YES,LFFA_TEST_MODE:YES,MACAN:A2,MACAN_I2C_MASK,RT13:B1_DEV,USBCPC:ROM3,USBC_DUAL_KIS:YES</td></tr><tr><td>X2523_FWR</td><td colspan="3">PFW2_DSCMG,PSVUSB_DSCMG,X2523_AUSTRINGER,X2523_ICEMAN,X2523_MAVERICKS,X2523_MIRABEAU,X2523_WHAMOLA</td></tr><tr><td>X2523_AUSTRINGER</td><td colspan="3">AUSTRINGER:A1_0_3PH_SPM,EXARA:A1</td></tr><tr><td>X2523_ICEMAN</td><td colspan="3">P3V5ACN_IC:A2_R170,P3V5ACN_LPM,P3V5ELIM:BOCM_SV</td></tr><tr><td>X2523_MAVERICKS</td><td colspan="3">MVR_OTP:FJ,FBUS:3S,PM32K:OSC_QRTZ</td></tr><tr><td>X2523_MIRABEAU</td><td colspan="3"></td></tr><tr><td>X2523_WHAMOLA</td><td colspan="3">WHAMOLA:0A936,SV8_DLY:YES,CNDR_DCINCAP1,CNDR_DCINCAP2</td></tr></table>				BOM GROUP	BOM OPTIONS			X2523_COMMON	SCH,PCB,COMMON,ALT_CM,ALTERNATE:INSTANCE,X2523_COMMON1,X2523_COMMON2,X2523_PROGPARTS,X2523_BLC,X2523_BOS,X2523_HDMI,X2523_SOC,X2523_USBC,X2523_FWR			X2523_COMMON1	BOARD_ID,BOARD_REV:0011,BOOTCFG2			X2523_COMMON2	RF_CONN,REFIDU_IC:HMI286,BTFNR,VITAMIN-C:NG			X2523_PROGPARTS	ATCCTR_BOM:WINBOND,ACE_ROM:V3_011,HDMI_ROM:FREEP			X2523_BLC	BLC_BEN_IC:V4,BLC_SV_SERIES:I10_OHM,BLC_SV_CAP:4P7_UF			X2523_BOS	BOS:B1_DEV			X2523_HDMI	CONRA:CFG2,CONRAPART:0,DATA_FILT,HDMI_CLC_FILT:YES,LDO_HDMI:SV			X2523_SOC	DRAMST:PMIO,VDDIEM:1777			X2523_USBC	ACE_WILL_BE_OTFED:YES,LFFA_TEST_MODE:YES,MACAN:A2,MACAN_I2C_MASK,RT13:B1_DEV,USBCPC:ROM3,USBC_DUAL_KIS:YES			X2523_FWR	PFW2_DSCMG,PSVUSB_DSCMG,X2523_AUSTRINGER,X2523_ICEMAN,X2523_MAVERICKS,X2523_MIRABEAU,X2523_WHAMOLA			X2523_AUSTRINGER	AUSTRINGER:A1_0_3PH_SPM,EXARA:A1			X2523_ICEMAN	P3V5ACN_IC:A2_R170,P3V5ACN_LPM,P3V5ELIM:BOCM_SV			X2523_MAVERICKS	MVR_OTP:FJ,FBUS:3S,PM32K:OSC_QRTZ			X2523_MIRABEAU				X2523_WHAMOLA	WHAMOLA:0A936,SV8_DLY:YES,CNDR_DCINCAP1,CNDR_DCINCAP2			<table><tr><th>BOM NUMBER</th><th colspan="2">BOM NAME</th><th colspan="2">BOM OPTIONS</th></tr><tr><td>685-00457</td><td colspan="2">COMMON BOM,MLB-S,X2523</td><td colspan="2">X2523_COMMON</td></tr><tr><td>985-01700</td><td colspan="2">DEV BOM,MLB-S,X2523</td><td colspan="2">X2523_DEVEL:ENG</td></tr></table>				BOM NUMBER	BOM NAME		BOM OPTIONS		685-00457	COMMON BOM,MLB-S,X2523		X2523_COMMON		985-01700	DEV BOM,MLB-S,X2523		X2523_DEVEL:ENG
BOM GROUP	BOM OPTIONS																																																																																					
X2523_COMMON	SCH,PCB,COMMON,ALT_CM,ALTERNATE:INSTANCE,X2523_COMMON1,X2523_COMMON2,X2523_PROGPARTS,X2523_BLC,X2523_BOS,X2523_HDMI,X2523_SOC,X2523_USBC,X2523_FWR																																																																																					
X2523_COMMON1	BOARD_ID,BOARD_REV:0011,BOOTCFG2																																																																																					
X2523_COMMON2	RF_CONN,REFIDU_IC:HMI286,BTFNR,VITAMIN-C:NG																																																																																					
X2523_PROGPARTS	ATCCTR_BOM:WINBOND,ACE_ROM:V3_011,HDMI_ROM:FREEP																																																																																					
X2523_BLC	BLC_BEN_IC:V4,BLC_SV_SERIES:I10_OHM,BLC_SV_CAP:4P7_UF																																																																																					
X2523_BOS	BOS:B1_DEV																																																																																					
X2523_HDMI	CONRA:CFG2,CONRAPART:0,DATA_FILT,HDMI_CLC_FILT:YES,LDO_HDMI:SV																																																																																					
X2523_SOC	DRAMST:PMIO,VDDIEM:1777																																																																																					
X2523_USBC	ACE_WILL_BE_OTFED:YES,LFFA_TEST_MODE:YES,MACAN:A2,MACAN_I2C_MASK,RT13:B1_DEV,USBCPC:ROM3,USBC_DUAL_KIS:YES																																																																																					
X2523_FWR	PFW2_DSCMG,PSVUSB_DSCMG,X2523_AUSTRINGER,X2523_ICEMAN,X2523_MAVERICKS,X2523_MIRABEAU,X2523_WHAMOLA																																																																																					
X2523_AUSTRINGER	AUSTRINGER:A1_0_3PH_SPM,EXARA:A1																																																																																					
X2523_ICEMAN	P3V5ACN_IC:A2_R170,P3V5ACN_LPM,P3V5ELIM:BOCM_SV																																																																																					
X2523_MAVERICKS	MVR_OTP:FJ,FBUS:3S,PM32K:OSC_QRTZ																																																																																					
X2523_MIRABEAU																																																																																						
X2523_WHAMOLA	WHAMOLA:0A936,SV8_DLY:YES,CNDR_DCINCAP1,CNDR_DCINCAP2																																																																																					
BOM NUMBER	BOM NAME		BOM OPTIONS																																																																																			
685-00457	COMMON BOM,MLB-S,X2523		X2523_COMMON																																																																																			
985-01700	DEV BOM,MLB-S,X2523		X2523_DEVEL:ENG																																																																																			
C	DEV BOM GROUPS				Variable BOM Groups/Development/Base BOMs																																																																																	
	<table><tr><th>BOM GROUP</th><th colspan="3">BOM OPTIONS</th></tr><tr><td>X2523_DEVEL:ENG</td><td colspan="3">ALTERNATE:INSTANCE,ALT_CM,AMP_DEV,BATT_OHG,DRG_RTH,DRG_LED,DEV_FPD,DRGSS_DEV,USBC_DRG,WEAT_DRG</td></tr><tr><td>X2523_DEVEL:PVT</td><td colspan="3">ALTERNATE:INSTANCE,USBC_DRG</td></tr></table>				BOM GROUP	BOM OPTIONS			X2523_DEVEL:ENG	ALTERNATE:INSTANCE,ALT_CM,AMP_DEV,BATT_OHG,DRG_RTH,DRG_LED,DEV_FPD,DRGSS_DEV,USBC_DRG,WEAT_DRG			X2523_DEVEL:PVT	ALTERNATE:INSTANCE,USBC_DRG			<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>685-00457</td><td>1</td><td>COMMON BOM,MLB-S,X2523</td><td>BASE</td><td>CRITICAL</td><td>BASE_BOM</td></tr><tr><td>985-01700</td><td>1</td><td>DEV BOM,MLB-S,X2523</td><td>DEVEL</td><td>CRITICAL</td><td>DEVEL_BOM</td></tr></table>				PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	685-00457	1	COMMON BOM,MLB-S,X2523	BASE	CRITICAL	BASE_BOM	985-01700	1	DEV BOM,MLB-S,X2523	DEVEL	CRITICAL	DEVEL_BOM																																																
BOM GROUP	BOM OPTIONS																																																																																					
X2523_DEVEL:ENG	ALTERNATE:INSTANCE,ALT_CM,AMP_DEV,BATT_OHG,DRG_RTH,DRG_LED,DEV_FPD,DRGSS_DEV,USBC_DRG,WEAT_DRG																																																																																					
X2523_DEVEL:PVT	ALTERNATE:INSTANCE,USBC_DRG																																																																																					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																	
685-00457	1	COMMON BOM,MLB-S,X2523	BASE	CRITICAL	BASE_BOM																																																																																	
985-01700	1	DEV BOM,MLB-S,X2523	DEVEL	CRITICAL	DEVEL_BOM																																																																																	
B	BOARD REV BOM				SSD 685 BOM Variants																																																																																	
	<table><tr><th>BOM GROUP</th><th colspan="3">BOM OPTIONS</th></tr><tr><td>BOARD_REV:1111</td><td colspan="3"></td></tr><tr><td>BOARD_REV:1110</td><td colspan="3">BOARDREV0</td></tr><tr><td>BOARD_REV:1101</td><td colspan="3">BOARDREV1</td></tr><tr><td>BOARD_REV:1000</td><td colspan="3">BOARDREV2,BOARDREV1,BOARDREV0</td></tr><tr><td>BOARD_REV:0111</td><td colspan="3">BOARDREV3</td></tr><tr><td>BOARD_REV:0110</td><td colspan="3">BOARDREV3,BOARDREV0</td></tr><tr><td>BOARD_REV:0100</td><td colspan="3">BOARDREV3,BOARDREV1,BOARDREV0</td></tr><tr><td>BOARD_REV:0011</td><td colspan="3">BOARDREV3,BOARDREV2</td></tr><tr><td>BOARD_REV:0001</td><td colspan="3">BOARDREV3,BOARDREV2,BOARDREV1</td></tr><tr><td>BOARD_REV:0000</td><td colspan="3">BOARDREV3,BOARDREV2,BOARDREV1,BOARDREV0</td></tr></table> https://compass.scv.apple.com/confluence/pages/viewpage.action?spaceKey=kalamataMSE&title=41x8+Revs				BOM GROUP	BOM OPTIONS			BOARD_REV:1111				BOARD_REV:1110	BOARDREV0			BOARD_REV:1101	BOARDREV1			BOARD_REV:1000	BOARDREV2,BOARDREV1,BOARDREV0			BOARD_REV:0111	BOARDREV3			BOARD_REV:0110	BOARDREV3,BOARDREV0			BOARD_REV:0100	BOARDREV3,BOARDREV1,BOARDREV0			BOARD_REV:0011	BOARDREV3,BOARDREV2			BOARD_REV:0001	BOARDREV3,BOARDREV2,BOARDREV1			BOARD_REV:0000	BOARDREV3,BOARDREV2,BOARDREV1,BOARDREV0			<table><tr><th>BOM NUMBER</th><th colspan="2">BOM NAME</th><th colspan="2">BOM OPTIONS</th></tr><tr><td>685-00493</td><td colspan="2">COMMON BOM,SSD_2 LAND,MLB-S,X2523</td><td colspan="2">ALT_CM,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L2</td></tr><tr><td>685-00458</td><td colspan="2">COMMON BOM,SSD_4 LAND,MLB-S,X2523</td><td colspan="2">ALT_CM,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L4</td></tr><tr><td>685-00460</td><td colspan="2">COMMON BOM,SSD_8 LAND,MLB-S,X2523</td><td colspan="2">ALT_CM,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L8</td></tr></table>				BOM NUMBER	BOM NAME		BOM OPTIONS		685-00493	COMMON BOM,SSD_2 LAND,MLB-S,X2523		ALT_CM,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L2		685-00458	COMMON BOM,SSD_4 LAND,MLB-S,X2523		ALT_CM,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L4		685-00460	COMMON BOM,SSD_8 LAND,MLB-S,X2523		ALT_CM,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L8															
BOM GROUP	BOM OPTIONS																																																																																					
BOARD_REV:1111																																																																																						
BOARD_REV:1110	BOARDREV0																																																																																					
BOARD_REV:1101	BOARDREV1																																																																																					
BOARD_REV:1000	BOARDREV2,BOARDREV1,BOARDREV0																																																																																					
BOARD_REV:0111	BOARDREV3																																																																																					
BOARD_REV:0110	BOARDREV3,BOARDREV0																																																																																					
BOARD_REV:0100	BOARDREV3,BOARDREV1,BOARDREV0																																																																																					
BOARD_REV:0011	BOARDREV3,BOARDREV2																																																																																					
BOARD_REV:0001	BOARDREV3,BOARDREV2,BOARDREV1																																																																																					
BOARD_REV:0000	BOARDREV3,BOARDREV2,BOARDREV1,BOARDREV0																																																																																					
BOM NUMBER	BOM NAME		BOM OPTIONS																																																																																			
685-00493	COMMON BOM,SSD_2 LAND,MLB-S,X2523		ALT_CM,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L2																																																																																			
685-00458	COMMON BOM,SSD_4 LAND,MLB-S,X2523		ALT_CM,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L4																																																																																			
685-00460	COMMON BOM,SSD_8 LAND,MLB-S,X2523		ALT_CM,ALTERNATE:INSTANCE,SSD_SUPPORT:L1-L8																																																																																			
A	BOARD ID				SSD Variable BOM Groups/Development																																																																																	
	<table><tr><th>BOM GROUP</th><th colspan="3">BOM OPTIONS</th></tr><tr><td>BOARD_ID</td><td colspan="3">BOARDID2</td></tr></table> For X2523 use BOARD_ID[7:0] = 0000010x rdar:///74602645 (Board IDs for Rhodes Macs)				BOM GROUP	BOM OPTIONS			BOARD_ID	BOARDID2			<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>685-00493</td><td>1</td><td>SSD PARTS,SSD_2 LAND,MLB-S,X2523</td><td>SSD</td><td>CRITICAL</td><td>LND_2_BOM</td></tr><tr><td>685-00458</td><td>1</td><td>SSD PARTS,SSD_4 LAND,MLB-S,X2523</td><td>SSD</td><td>CRITICAL</td><td>LND_4_BOM</td></tr><tr><td>685-00460</td><td>1</td><td>SSD PARTS,SSD_8 LAND,MLB-S,X2523</td><td>SSD</td><td>CRITICAL</td><td>LND_8_BOM</td></tr></table>				PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	685-00493	1	SSD PARTS,SSD_2 LAND,MLB-S,X2523	SSD	CRITICAL	LND_2_BOM	685-00458	1	SSD PARTS,SSD_4 LAND,MLB-S,X2523	SSD	CRITICAL	LND_4_BOM	685-00460	1	SSD PARTS,SSD_8 LAND,MLB-S,X2523	SSD	CRITICAL	LND_8_BOM																																														
BOM GROUP	BOM OPTIONS																																																																																					
BOARD_ID	BOARDID2																																																																																					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																	
685-00493	1	SSD PARTS,SSD_2 LAND,MLB-S,X2523	SSD	CRITICAL	LND_2_BOM																																																																																	
685-00458	1	SSD PARTS,SSD_4 LAND,MLB-S,X2523	SSD	CRITICAL	LND_4_BOM																																																																																	
685-00460	1	SSD PARTS,SSD_8 LAND,MLB-S,X2523	SSD	CRITICAL	LND_8_BOM																																																																																	
A	SSD Support BOM Groups				BOM GROUPS																																																																																	
	<table><tr><th>BOM GROUP</th><th>Host BOM</th><th colspan="3">BOM OPTIONS</th></tr><tr><td>SSD_SUPPORT:L1-L2</td><td>2L Support BOM</td><td colspan="3">SSD_2L</td></tr><tr><td>SSD_SUPPORT:L1-L4</td><td>4L Support BOM</td><td colspan="3">SSD_2L,SSD_4L,SSD_BRANCH_2L</td></tr><tr><td>SSD_SUPPORT:L1-L8</td><td>8L Support BOM</td><td colspan="3">SSD_2L,SSD_4L,SSD_OC1VR1,SSD_8L,SSD_BRANCH_2L</td></tr></table>				BOM GROUP	Host BOM	BOM OPTIONS			SSD_SUPPORT:L1-L2	2L Support BOM	SSD_2L			SSD_SUPPORT:L1-L4	4L Support BOM	SSD_2L,SSD_4L,SSD_BRANCH_2L			SSD_SUPPORT:L1-L8	8L Support BOM	SSD_2L,SSD_4L,SSD_OC1VR1,SSD_8L,SSD_BRANCH_2L			<table><tr><th>DOCUMENT NUMBER</th><th>DATE</th></tr><tr><td>051-08012</td><td>D</td></tr><tr><th>REVISION</th><td>4.0.0</td></tr><tr><th>ISSUANCE</th><td>evt-1</td></tr><tr><th>PAGES</th><td>602 OF 700</td></tr><tr><th>SHEET</th><td>155 OF 159</td></tr></table>				DOCUMENT NUMBER	DATE	051-08012	D	REVISION	4.0.0	ISSUANCE	evt-1	PAGES	602 OF 700	SHEET	155 OF 159																																														
BOM GROUP	Host BOM	BOM OPTIONS																																																																																				
SSD_SUPPORT:L1-L2	2L Support BOM	SSD_2L																																																																																				
SSD_SUPPORT:L1-L4	4L Support BOM	SSD_2L,SSD_4L,SSD_BRANCH_2L																																																																																				
SSD_SUPPORT:L1-L8	8L Support BOM	SSD_2L,SSD_4L,SSD_OC1VR1,SSD_8L,SSD_BRANCH_2L																																																																																				
DOCUMENT NUMBER	DATE																																																																																					
051-08012	D																																																																																					
REVISION	4.0.0																																																																																					
ISSUANCE	evt-1																																																																																					
PAGES	602 OF 700																																																																																					
SHEET	155 OF 159																																																																																					
				Apple Inc.																																																																																		
				NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE RECIPIENT AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2 NOT TO REPRODUCE OR COPY IT 3 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4 ALL RIGHTS RESERVED																																																																																		

BOM VARIANT TABLES

BOM NUMBER	BOM NAME	BOM OPTIONS
------------	----------	-------------

P1S

639-16889	MLB_S,8C,16G,19FSTP,1TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:1TB_KX
639-16890	MLB_S,8C,32G,19FSTP,1TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:1TB_KX
639-16891	MLB_S,8C,16G,19FSTP,4TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:4TB_KX
639-16892	MLB_S,8C,32G,19FSTP,4TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:4TB_KX
639-16893	MLB_S,8C,16G,19FSTP,8TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:8TB_KX
639-16894	MLB_S,8C,32G,19FSTP,8TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:8TB_KX

639-16905	MLB_S,6C,16G,16FSTP,1TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:1TB_KX
639-16906	MLB_S,6C,32G,16FSTP,1TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:1TB_KX
639-16907	MLB_S,6C,16G,16FSTP,4TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:4TB_KX
639-16908	MLB_S,6C,32G,16FSTP,4TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:4TB_KX
639-16909	MLB_S,6C,16G,16FSTP,8TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:8TB_KX
639-16910	MLB_S,6C,32G,16FSTP,8TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:8TB_KX

639-17289	MLB_S,8C,16G,19FSTP,1TB_HY,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:1TB_HY
639-17290	MLB_S,8C,32G,19FSTP,1TB_HY,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:1TB_HY
639-17291	MLB_S,8C,16G,19FSTP,2TB_HY,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:2TB_HY
639-17292	MLB_S,8C,32G,19FSTP,2TB_HY,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:2TB_HY
639-17293	MLB_S,8C,16G,19FSTP,4TB_WD,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:4TB_WD
639-17294	MLB_S,8C,32G,19FSTP,4TB_WD,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:4TB_WD
639-17295	MLB_S,8C,16G,19FSTP,8TB_WD,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:8TB_WD
639-17296	MLB_S,8C,32G,19FSTP,8TB_WD,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:8TB_WD

639-17305	MLB_S,6C,16G,16FSTP,1TB_HY,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:1TB_HY
639-17306	MLB_S,6C,32G,16FSTP,1TB_HY,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:1TB_HY
639-17307	MLB_S,6C,16G,16FSTP,2TB_HY,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:2TB_HY
639-17308	MLB_S,6C,32G,16FSTP,2TB_HY,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:2TB_HY
639-17309	MLB_S,6C,16G,16FSTP,4TB_WD,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:4TB_WD
639-17310	MLB_S,6C,32G,16FSTP,4TB_WD,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:4TB_WD
639-17311	MLB_S,6C,16G,16FSTP,8TB_WD,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:8TB_WD
639-17312	MLB_S,6C,32G,16FSTP,8TB_WD,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:8TB_WD

BOM VARIANT TABLES

BOM NUMBER	BOM NAME	BOM OPTIONS
------------	----------	-------------

939-13297	MLB_S,DCDC1,SOC_SOCKET,SSD_SOCKET,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:SOCKET,SSD:SOCKET
939-13298	MLB_S,DCDC2,NO_SOC,NO_SSD_SOCKET,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SSD:NOISE

512G 2 LANDINGS NAND-KX

639-17088	MLB_S,8C,16G,19FSTP,512G_KX-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:512GB_KX_2L
639-17089	MLB_S,8C,32G,19FSTP,512G_KX-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:512GB_KX_2L
639-16936	MLB_S,6C,16G,16FSTP,512G_KX-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:512GB_KX_2L
639-16937	MLB_S,6C,32G,16FSTP,512G_KX-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:512GB_KX_2L

2TB NAND

639-16960	MLB_S,8C,16G,19FSTP,2TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:2TB_KX
639-16961	MLB_S,8C,32G,19FSTP,2TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:2TB_KX
639-16964	MLB_S,6C,16G,16FSTP,2TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:2TB_KX
639-16965	MLB_S,6C,32G,16FSTP,2TB_TS,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:2TB_KX

512G 2 landings NAND- HYNIX

639-16993	MLB_S,8C,16G,19FSTP,512G_HY-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:512GB_HY_2L
639-16994	MLB_S,8C,32G,19FSTP,512G_HY-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:512GB_HY_2L
639-16997	MLB_S,6C,16G,16FSTP,512G_HY-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:512GB_HY_2L
639-16998	MLB_S,6C,32G,16FSTP,512G_HY-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:512GB_HY_2L

512G 2 landings NAND- WD

639-17082	MLB_S,8C,16G,19FSTP,512G_WD-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_16G,88D:512GB_WD_2L
639-17083	MLB_S,8C,32G,19FSTP,512G_WD-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:8C,19FSTP_32G,88D:512GB_WD_2L
639-17086	MLB_S,6C,16G,16FSTP,512G_WD-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_16G,88D:512GB_WD_2L
639-17087	MLB_S,6C,32G,16FSTP,512G_WD-2L,X2523	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:6C,16FSTP_32G,88D:512GB_WD_2L

BOM VARIANT TABLES		
 Apple Inc.	REVISION NUMBER	PAGE
	051-08012	D
	4.0.0	
	DATE	evt-1
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE READER AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED		603 OF 700
		156 OF 159

8	7	6	5	4	3	2	1
BOM VARIANT TABLES				BOM VARIANT TABLES			
BOM NUMBER		BOM NAME		BOM OPTIONS			
BOM VARIANT TABLES-P1,P2				BOM VARIANT TABLES-P1,P2			

[illegible]

[illegible]